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Efficiency Comparison of Asynchronous and Synchronous Buck Converter with Variation in Duty Cycle and Output Current

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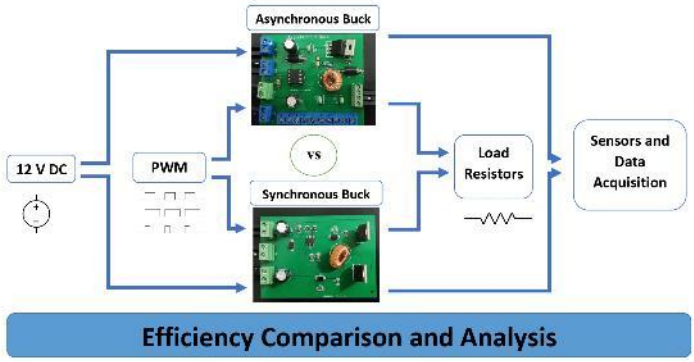
ABSTRACT



There are two most commonly used topologies in buck converter applications, asynchronous and synchronous buck converter. These two topologies have its own advantages and disadvantages from a performance point of view. The difference in performance, especially in the aspect of efficiency need to be addressed further, knowing the efficiency is a crucial aspect of buck converter application. In this study, the comparison of asynchronous and synchronous topology in terms of its efficiency will be analyzed using software simulation and hardware prototypes. Software simulation will be used to validate the workings of buck converter prototypes by comparing its characteristics against the hardware prototypes. Furthermore, the performance between both topologies will be analyzed under various operating conditions. Based on the results obtained in this study, when the applied duty cycle is low, for instance in 30% duty cycle and both converters operate at the lowest current, the asynchronous topology have a better efficiency of 19.15% against the synchronous topology, however, when both converters operate at the highest current, the synchronous topology shows its efficiency advantage of 6.56% against the asynchronous topology. On the other hand, in a higher duty cycle operation, for example in 80% duty cycle, both converters have an insignificant difference of efficiency.

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1. INTRODUCTION

Electronics based technology is increasing in terms of its quantity and can be found in many aspects of our lives. Over the last few years, we can see the rapid development of portable electronics devices used by our society in terms of its performance or the number of its users. Those devices include smartphones, smart watches, tablets, notebooks, or even a very portable devices such as wireless earphones[1], [2]. All those devices require electrical power either directly or in the form of a battery. Power requirements will lead to a power conversion system or converter to regulate the amount of voltage applied to those devices from our electrical sources[3]–[5] Power conversion system is a crucial part of portable electronic device operation and can impact positively on device efficiency, allowing smaller form factor and longer battery life[6]–[9].

An efficient power conversion system can be achieved using the application of switched mode DC-DC converter[10]–[12]. With its switching methods, the switched mode DC-DC converter can be considered as a Switch Mode Power Supply (SMPS), specifically a type of power supply that uses a high frequency square wave or a pulse width modulation signal for driving an electronic switch[13]. The use of this method can achieve a range of efficiencies higher than a simpler linear power supply[14]. One kind of DC-DC converter is a buck converter that can lower a voltage source to a desired level of regulated voltage output using the adjustment of Pulse Width Modulation duty cycle applied to the switching transistor[15]–[21].

To achieve the aforementioned switching method for buck converter, there are two kinds of switches in the converter, a high side switch and a low side switch. Both switches conduct alternately with each other in its operation. For an asynchronous buck converter, to achieve alternate conduction, a MOSFET as a high side switch and a diode as a low side switch were used, whereas a synchronous buck converter will use a MOSFET for both switches[22]. One of the advantages of using MOSFET as a low side switch is its low on resistance and a MOSFET does not have a forward voltage drop as in a diode[23]–[25] Besides the advantages of using MOSFET for both switches, a more complex switching mechanism is required for the synchronous buck converter. The asynchronous topology only needs one PWM signal to drive the high-side MOSFET, whereas the synchronous topology needs two PWM signals that alternate with each other to drive both the high-side and low-side MOSFETs[26].

An efficiency comparison between the asynchronous and synchronous topologies is needed to further analyze each topology advantage under various operating conditions. Previous research of the two topologies has been conducted with various forms of analysis in different aspects. There has been research that compares the efficiency of asynchronous and synchronous topologies[27]–[29] and also research that analyzed the effect of resistive load[30], [31].

This study will be conducted by not only designing the software simulation model but also designing the hardware prototypes of asynchronous and synchronous buck converter. The converters will be experimented under various operating conditions by varying the duty cycle and the load resistance. In each operating condition, the conversion efficiency of both converters in both software simulation and hardware prototypes will be acquired. The efficiency of software simulation and hardware prototypes will be compared as a means to validate the workings of the designed buck converters. Furthermore, the main contribution of this study is comparative efficiency analysis between the asynchronous and synchronous topologies prototypes to analyze the performance of the proposed buck converters under various operating conditions.

2. BUCK CONVERTER TOPOLOGY

Buck Converters has a lesser average voltage output than its input voltage[32]. This drop in voltage was the result of an inductor component in a buck converter when it was operated in two states, the off state and the on state[33]. These two states of the buck converter can occur because of the presence of two switches, a low-side switch and a high-side switch. These two switches will also differentiate between the topologies of buck converters that will present in this research, an asynchronous buck converter and a synchronous buck converter. The two topologies will use a MOSFET for the high side switch application, but for the low side switch, the asynchronous buck converter uses a flyback diode, whereas the synchronous buck converter uses a MOSFET[34]. This difference in the choice of component will results in a different switching mechanism, where an asynchronous buck only needs one PWM signal to drive the high-side MOSFET, while a synchronous buck will need two PWM signals to drive both switches.

Besides the switching mechanism, the differences in power loss will also occurs due to the different use of components. Diodes generally tend to have a relatively high power loss, while MOSFETs will have a lower power loss compared to diodes when in conduction[35]. This power loss will impact the efficiency of the buck converter as a whole. Figure 1 will show a simplified version of both buck converter topologies.

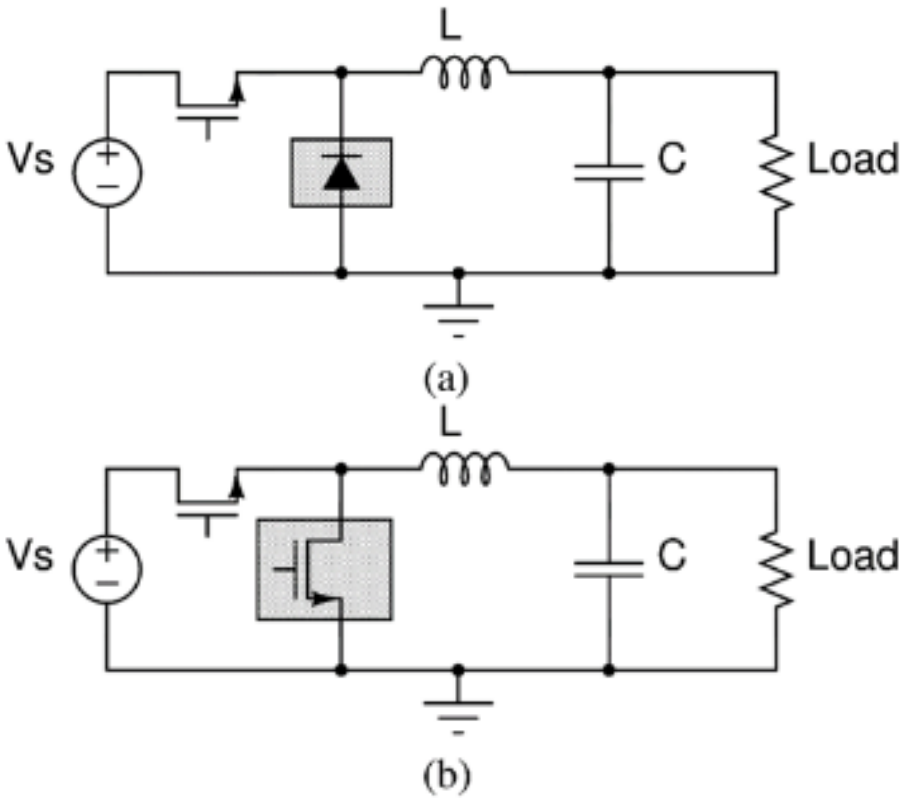

Figure 1. Simplified Version of Buck Converter: (a) Asynchronous Buck Converter (b) Synchronous Buck Converter

The two states of buck converter operation will define the working principle of the buck converter. Firstly, the on state of the buck converter will be represented in Figure 2, where the high-side switch is currently closed while the low side switch is open, so that there will be a current passing through the inductor, capacitor, and the load[36]. This condition is where the inductor will be connected to the source voltage and because of the voltage difference between the input and the output voltage, the current in the inductor is increasing[37]. The inductor current will pass through the output capacitor and the load[37]. Because of the current flow, the inductor will store energy in the form of magnetic field. In the asynchronous buck converter where a flyback diode is used as a low side switch, the diode will operate in reverse bias and will not accommodate the flow of current[38], [39].

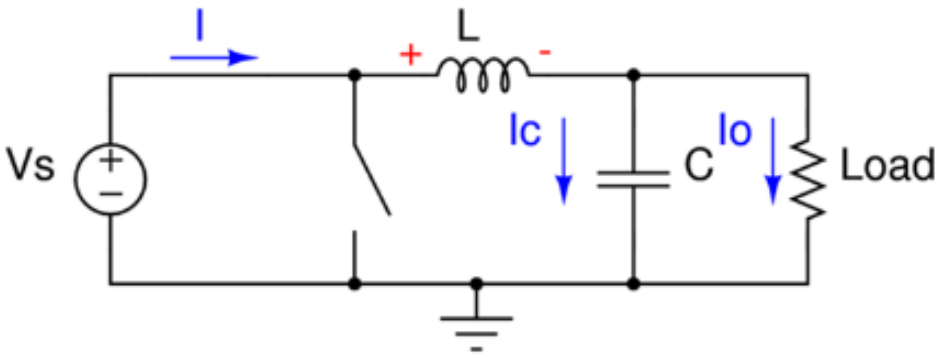

Figure 2. Buck Converter On State

When the buck converter is in the off state as in Figure 3, the high-side switch will open so that the voltage source is disconnected from the inductor. The low side switch is closed and will accommodate the flow of current from the inductor for transferring the energy stored by the inductor to the load[38]. In other words, in the off state, the inductor acts as a source and supply the current through the load resistor[20], [40]. The energy stored in the inductor and the current across it will decrease[40].

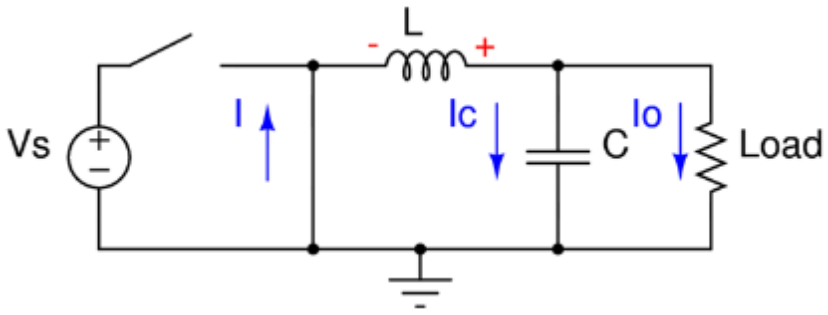

Figure 3. Buck Converter Off State

Based on the two state of buck converter operation, the synchronous buck converter, the two PWM signals that drive the MOSFET must be alternate to one another. When driving both MOSFETs alternately, because there is a rise and fall time of both MOSFETs, there is a possibility in which the high-side MOSFET and the low-side MOSFET active or conduct at the same time, or can be called as shoot-through[41], [42]. This will lead to the condition where current from the source voltage to flow through the ground with only a little resistance that exists on the two MOSFETs. Because of this condition, the rise and fall time of MOSFETs in use must be taken into consideration when driving both MOSFETs alternately. In this paper, a control system for PWM signals with built-in dead-time will be used for conquering this problem.

3. DESIGN PARAMETERS

The operational buck converter specification in this research is as seen in Table 1.

Table 1. Specification of the Buck Converter

Parameters	Value
Source Voltage	12 V
Maximum Current	5 A
Minimum Current	100 mA
Maximum Output Voltage	10.8 V
Duty Cycle Range	10% – 90%
Frequency	23 kHz
Voltage Ripple	5%
Current Ripple	20%

The components of buck converters such as: inductor, capacitor, MOSFET, and driver will be referred to the above specification. The two topologies of buck converters will have the same specification parameters, which leads to an identical values of components, such as inductance and capacitance. The difference between the two topologies is the use of MOSFET as a low side switch on the synchronous buck converter, whereas the asynchronous buck converter uses a Schottky diode and because of the different switching mechanism, there will be a different driver that controls the PWM signal of the MOSFET gate.

3.1. Input Capacitor

The input capacitance will be calculated according to the formula shown in the Equation (1), Equation (2), Equation (3).

$$C_{min} > \frac{(I_{out} + I_{minimum})}{8 \times fs \times V_{input\_ripple}} \quad (1)$$

$$C_{min} > \frac{(5 + 0.1)}{23 \times 10^{-3} \times 8 \times 0.6} \quad (2)$$

$$C_{min} > 46.1\ \mu F \quad (3)$$

The capacitance used will be set at 470 µF to further reduce ESR.

3.2. Output Capacitor

The output capacitor value will rely on the 20% current ripple value and the 5% ripple voltage value. The minimum output capacitor will be calculated as Equation (4), Equation (5) and Equation (6).

$$C_{min} > \frac{\Delta I_{Inductor}}{8 \times f_s \times \Delta V_{Output}} \quad (4)$$

$$C_{min} > \frac{0.2 \times 5}{8 \times 23 \times 10^3 \times 0.01 \times 10.8} \quad (5)$$

$$C_{min} > 50.322\ \mu F \quad (6)$$

To further reduce ESR, the output capacitance value of both converters is set at 470 µF.

3.3. Inductor

The inductance in the two topologies of buck converters will be set in 330 µH. Based on this value, the asynchronous buck converter will operate in Discontinuous Conduction Mode when a low current is given to the converter. Whereas the synchronous buck converter will always operate with Continuous Conduction Mode at any current because of its low side switch MOSFET.

3.4. MOSFET

IRFB3077PBF will be used for both topologies of the converter. To drive the floating high side switch, a single channel IR2117 driver is used for the asynchronous buck converter and a half-bridge driver IR2184 is used for the synchronous buck converter. In addition, IR2184 will also regulate the switching mechanism for driving the two MOSFETs alternately. To integrate both MOSFET drivers (IR2184 and IR2117) into the buck converter topology, a bootstrap circuit will be arranged so that both drivers can deliver a higher PWM signal (relative to the input PWM signal) for the high side switch MOSFETS of asynchronous and synchronous topology. The list of components used is shown in Table 2.

Table 2. List of Components

Component	Specification
Inductor	330 uH
Input Capacitor	470 µF
Output Capacitor	470 µF
MOSFET	IRFB3077PBF
Flyback Diode	1N5822

4. METHODS

The simulation model of the converters will be arranged in LTspice to validate and evaluate the workings of both topologies. Afterwards, the hardware prototype is assembled according to the simulation model. Mainly, the simulation model consists of 5 major parts, the buck converter itself, the voltage source, bootstrap and switching mechanism, PWM input as the switching signal, and the load resistance. The PWM input duty cycle and the load resistance will be varied within the LTspice program along with the measurement of input-output voltage and current in the varied condition. Efficiency results of both converters will also be calculated from the measured input-output voltage and current, also within the LTspice software. Figure 4 and Figure 5 will show the simulation model of asynchronous buck converter and synchronous buck converter, respectively.

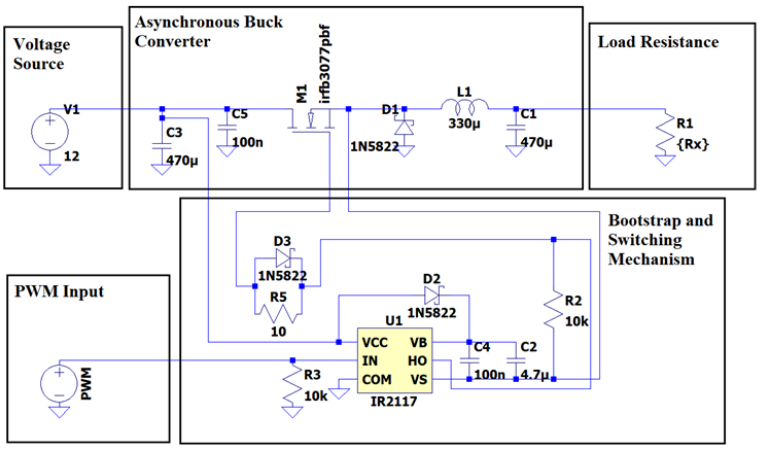

Figure 4. Simulation Model of Asynchronous Buck Converter

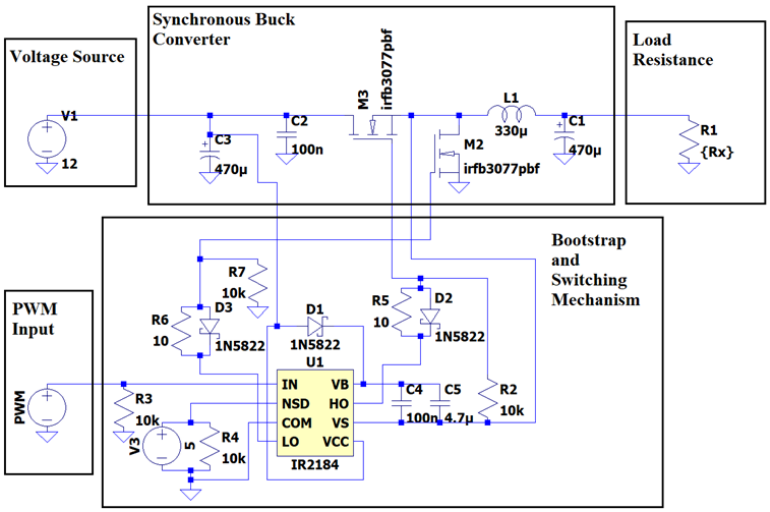

Figure 5. Simulation Model of Synchronous Buck Converter

The simulation model will be implemented into hardware prototypes for both converter topologies. The hardware protypes were a Printed Circuit Board as shown in the Figure 6 dan Figure 7 with the exact components and specification than that of the simulation model with the addition of some components for measurement and calculation of converter efficiency in various operating conditions. Same as the simulation model, the collected data in each experiment is in the form of input-output voltage and current. The measurement of voltage and current will be performed by two INA219 sensors, in which it will be placed between the input and output of both converters as done in previous research[43]. INA219 sensor will be integrated with Arduino microcontroller for collecting the measured data. The microcontroller will also calculate the efficiency measured in each measurement and display it in the LCD. Such method of using INA219 sensor for measuring voltage and current for both input and output terminal also found in previous research[44], in which INA 219 was used for measuring voltage and current in a solar cell application. The block diagram used for measurement in this study is shown in Figure 8.

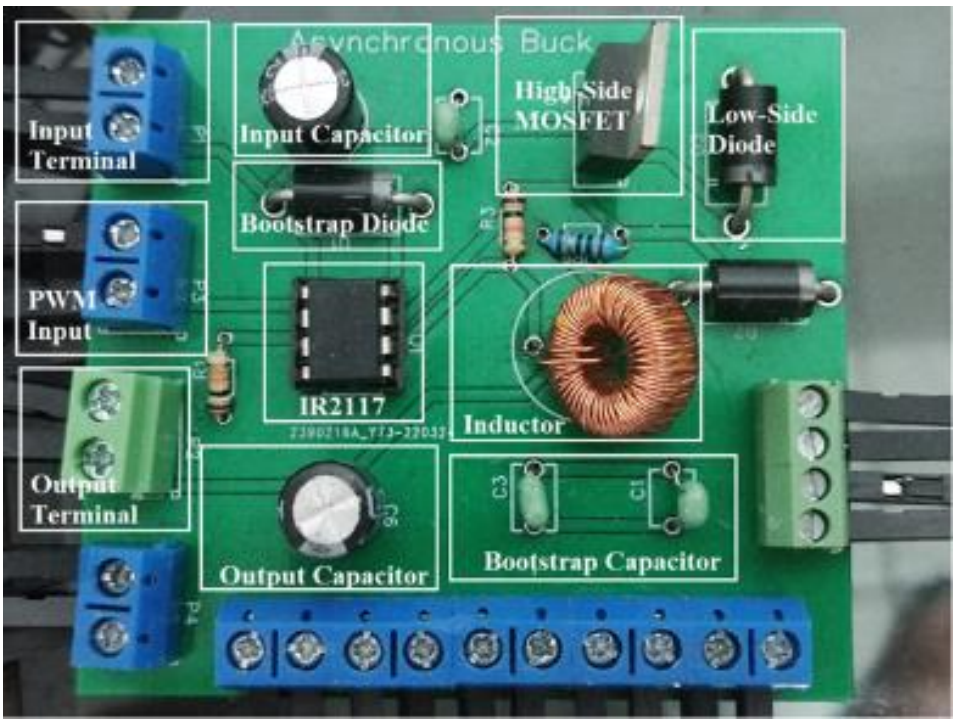

Figure 6. Asynchronous Buck Converters PCB Prototype

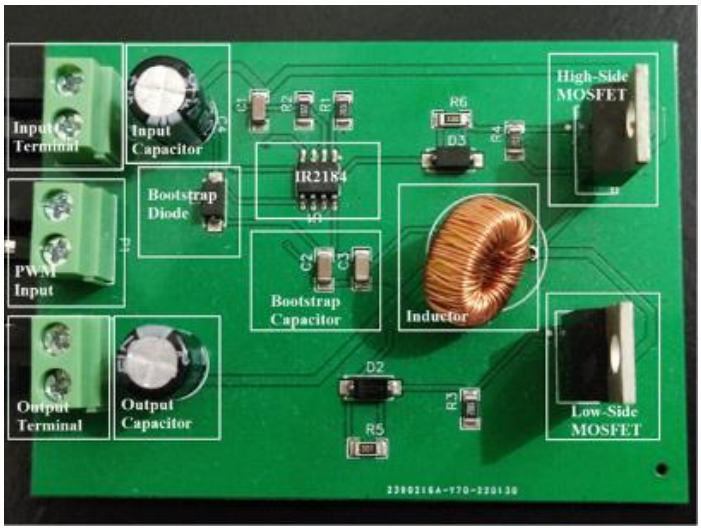

Figure 7. Synchronous Buck Converter PCB Prototype

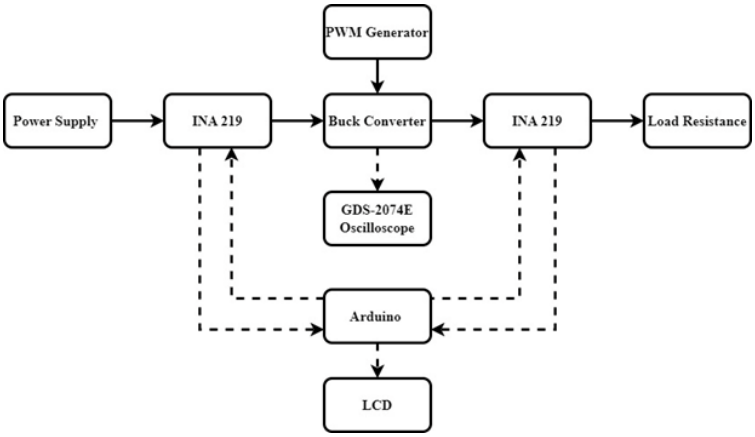

Figure 8. Block Diagram for Measurement

As for the data, firstly the switching mechanism of both converters will be analyzed by collecting voltage waveform data taken at its switch nodes using GW INSTEK GDS-2074E oscilloscope. Both converters will be experimented under varying current and duty cycles in each experiment. First stage of experiment aims to discover the effect of varying duty cycle by PWM generators in both converters, in which the converters will be connected to 33 Ω load resistance while the duty cycle is varied between 10 – 90% with 10% increment with each data retrieval. The second stage of experiment is more advanced with both converters experimented under varying duty cycle and the operation current. This stage of experiment will be divided under a low duty cycle application with 30% and 40% duty cycle applied to both converters and a high duty cycle application with 70% and 80% duty cycle. Thus, there will be 4 types of duty cycle variations applied to both converters and in each of the current variations will be varied with load resistance values between 56 Ω, 47 Ω, 33 Ω, 22 Ω,10 Ω, 8.2 Ω, 6.8 Ω, 5.6 Ω, 4.7 Ω, 3.3 Ω, and 2.2 Ω.

From this data, the efficiency can be acquired with firstly calculating the input and output power (P_{Input} and P_{Output}) using the Equation (7) an Equation (8).

$$P_{Input} = V_{Input} \times I_{Input} \tag{7}$$

$$P_{Output} = V_{Output} \times I_{Output} \tag{8}$$

After acquiring the input and output power, the efficiency will be calculated with a simple calculation as Equation (9).

$$Efficiency\ (\%) = \frac{P_{Output}}{P_{Input}} \times 100\% \tag{9}$$

5. RESULTS AND DISCUSSION

5.1. Switching Mechanism

Switching mechanism is a crucial factor in buck converter operation, either for synchronous topology or asynchronous topology. Figure 9 will show the voltage at the MOSFET gate of the asynchronous buck converter prototype during its operation. The figure was taken using GDS-2074E oscilloscope with 33 Ω connected to the load.

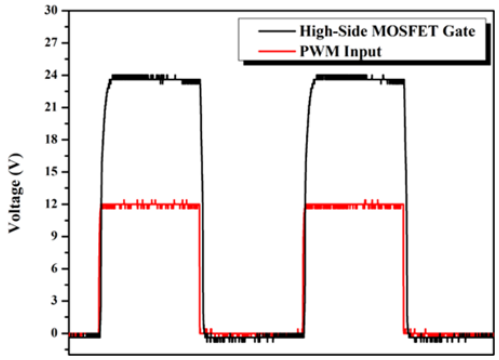

Figure 9. Asynchronous Buck Converter MOSFET Gate Voltage vs PWM input

Figure 9 shows the capability of the bootstrap circuit in the asynchronous buck converter for increasing the peak voltage from PWM input. The 12 V input will increase to around 24 V driving the MOSFET gate. The high on voltage is important in the buck converter operation because of the n-type MOSFET floating configuration.

Figure 10 shows the switching mechanism of the synchronous buck converter prototype connected to a 33 Ω load. Differ from the switching mechanism of asynchronous buck, the synchronous buck is more complex because of the low-side MOSFET existence. The two MOSFETs need to be conducted alternately so that there is a switchover from the on state to the off state as represented in Figure 10 (a). Figure 10 (b) shows the increased PWM input to around 22 V due to the bootstrap circuit mechanism for driving the high-side MOSFET.

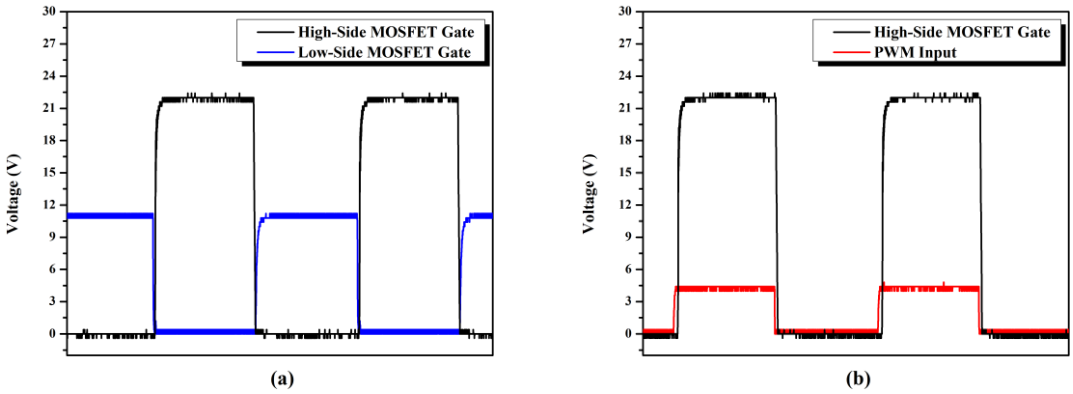

Figure 10. Synchronous Buck Converter Switching Mechanism: (a) High Side MOSFET Gate vs Low Side MOSFET Gate (b) High Side MOSFET Gate vs PWM Input

5.2. Efficiency Comparison of Simulation Model and Prototypes

The efficiency measurement for both buck converter topologies was conducted with the variation of duty cycle and load resistance. This research will acquire efficiency data from both simulation models and hardware prototypes. Efficiency results from the the simulation model can be used as a performance characteristic validation of the designed prototypes by analyzing the similarities and dissimilarities of characteristics between the simulation model and a real-life prototype. The simulations that has been conducted in LTspice software which does not factor in the dissipation that inevitably will happen in the wire and traces of prototypes. Comparison will be done for both duty cycle variation and load variation. The load variations will be divided into a low duty cycle application, and a high duty cycle application.

Figure 11 shows the comparison of efficiency results for both converter topologies with varying duty cycles. The figure shows a similar characteristic of efficiency between the simulation model and prototype.

However, the simulation models in both topologies have a higher efficiency value compared to those of the prototypes. This happens due to the effect of dissipation that was not calculated in the simulation models.

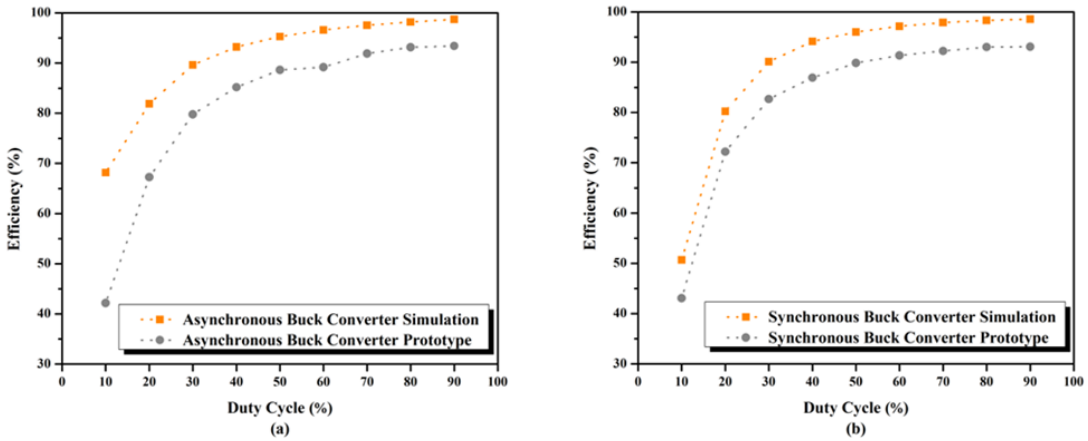

Figure 11. Efficiency Comparison Between Simulation and Prototype with Varying Duty Cycle: (a) Asynchronous Buck Converter (b) Synchronous Buck Converter

In a load variaton experiment with low duty cycle application also shows a similar characteristics in efficiency results for simulation model and prototype as shown in Figure 12. Higher efficiency value for simulation experiment is also shown in Figure 12.

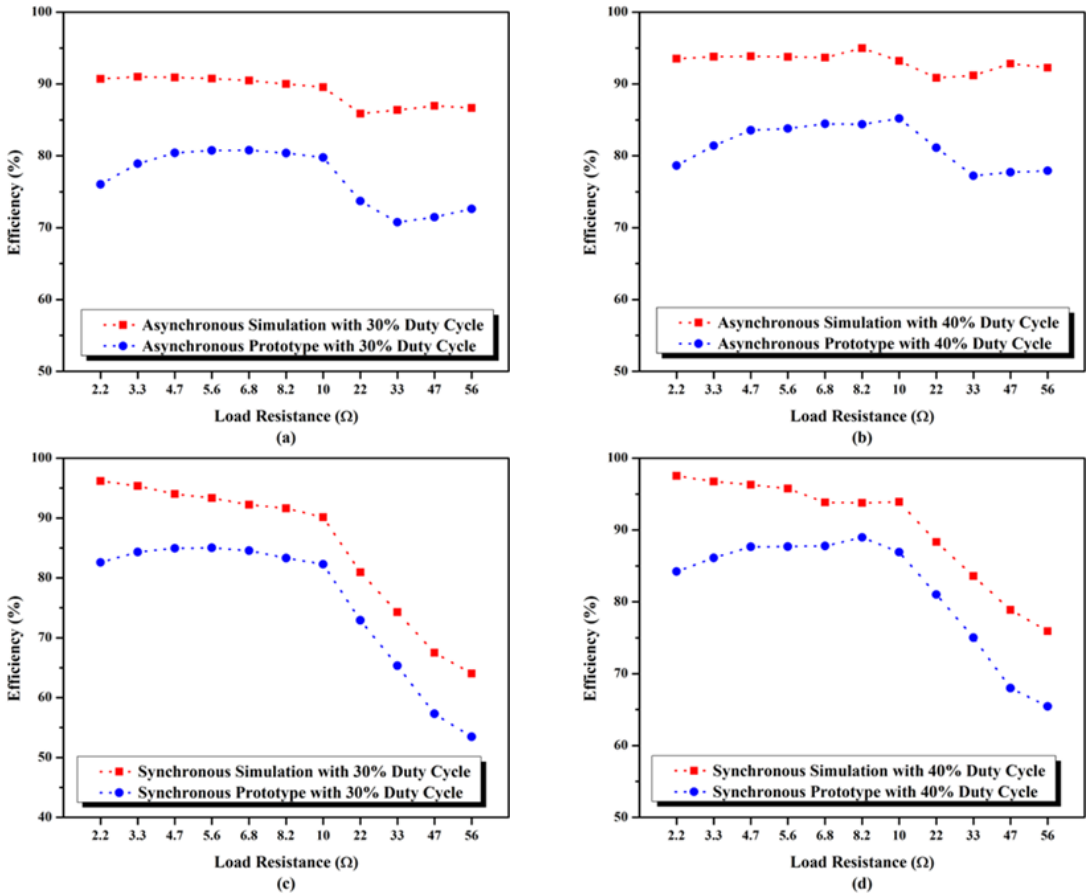

Figure 12. Efficiency Comparison Between Simulation and Prototype with Varying Load Resistance on a Low Duty Cycle Range: (a) Asynchronous Buck Converter with 30% Duty Cycle (b) Asynchronous Buck Converter with 40% Duty Cycle (c) Synchronous Buck Converter with 30% Duty Cycle (d) Synchronous Buck Converter with 40% Duty Cycle

For a higher duty cycle range, similar characteristics for efficiency were also occured as shown in Figure 13. Figure 13 also shows that in a high duty cycle range, the dissipation effect of the prototype is more prominent when the load resistance is small or a higher current operation, in which there is a more significant difference between the simulation and design simulation efficiency results. Despite the difference in overall efficiency value between the simulation model and prototype, the resemblance of efficiency results in terms of characteristics in a varying operating condition for both topologies concludes that the design prototypes successfully represent the conditions and characteristics of buck converters simulation model.

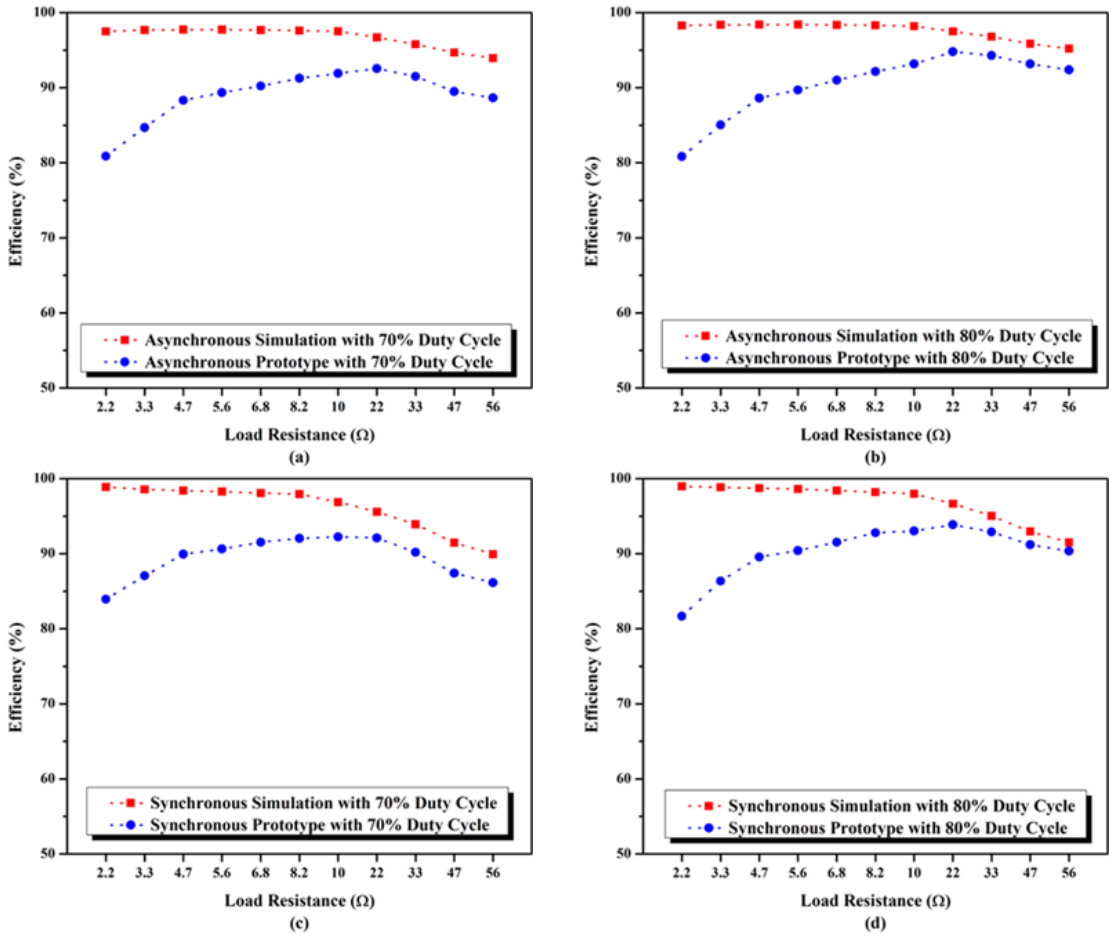

Figure 13. Efficiency Comparison Between Simulation and Prototype with Varying Load Resistance on a High Duty Cycle Range: (a) Asynchronous Buck Converter with 70% Duty Cycle (b) Asynchronous Buck Converter with 80% Duty Cycle (c) Synchronous Buck Converter with 70% Duty Cycle (d) Synchronous Buck Converter with 80% Duty Cycle

The major part of this research is analyzing the difference in efficiency results between an asynchronous buck converter and a synchronous buck converter. In this section, the performance in terms of power conversion efficiency for both topologies in various operating conditions will be discussed.

Figure 14 shows the efficiency results of both topologies with respect to duty cycle variation, in which the experiment was performed by connecting a constant 10 Ω resistance to the load. From Figure 14, it can be found that the efficiency value tends to increase along with the duty cycle. It can be analyzed that the quiescent current will have a significant impact on a lower duty cycle than a higher duty cycle because of the low input current. Besides that, the duty cycle determines the duration of conduction in the buck converter, a lower duty cycle value will cause the conduction time of low side switch to become longer than the high side switch, and vice versa for a higher duty cycle value. This difference in conduction time will have affected when comparing the two topologies. With a lower duty cycle value, the use of n-type MOSFETs for low-side switch in asynchronous topology compared to the use of Schottky diode in synchronous topology will have a significant impact on efficiency, the use of MOSFETs will make the converter more efficient because of the lower voltage drop than the diode.

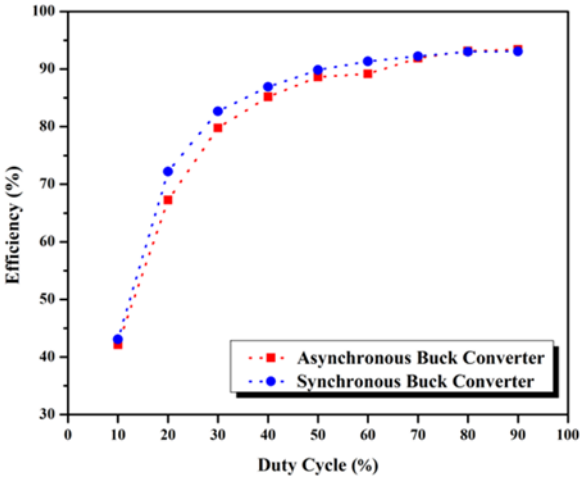

Figure 14. Duty Cycle Variation vs Converter Efficiency

To examine the efficiency comparison of the two topologies, further, the variation of load resistance is conducted, and due to the effect of duty cycle towards the conduction time, when conducting load variation experiment, this research will divide the fixed variable into a low duty cycle range which will be represented with 30% and 40% duty cycle and a high duty cycle range will be represented with 70% and 80% duty cycle. The load variation will represent the operating current of the buck converter. The higher load resistance values indicates the higher operating current and vice versa. An illustration of this result is shown in Figure 15.

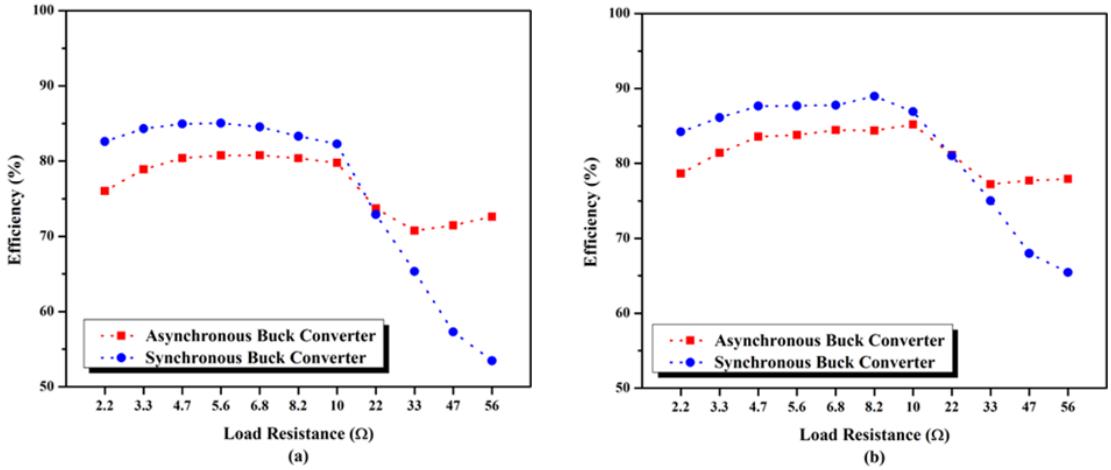

Figure 15. Load Resistance Variations on a Low Duty Cycle Range: (a) Prototype Experiment 30% Duty Cycle (b) Prototype Experiment 40% Duty Cycle

Generally, Figure 15 shows that both topologies have a low efficiency when the load resistance is high or in a low current operation. In a low current operation, the effect of quiescent current is more prominent because the difference between the quiescent current and input current is not significant. Besides that, the impact of conduction mode is also shown when the load is in the range of 22 Ω – 56 Ω. The synchronous topology that is conducted with CCM in that range of load resistance or low current operation will have a lower efficiency than that of the asynchronous topology that will conduct with DCM at low current operation. On the other hand, in the hardware experiment there is a slight decrease at higher current operation due to the more prominent dissipation. This dissipation can be seen when comparing between the two stages of experiment, with the simulation model showing no signs of dissipation.

As explained earlier, the lower duty cycle range also means that the low side switch conduction time will be longer than that of the high-side switch and can be seen in Figure 15, that the efficiency of synchronous buck converter is better at a load resistance that smaller than 22 Ω. This because the lower voltage drop of the n-type MSOFET on asynchronous topology compared to the voltage drop of Schottky diode on asynchronous topology has a significant impact on efficiency.

Figure 16 shows the load variations with a higher duty cycle range. In this range of duty cycles, the operational current for both topologies is higher than that of the lower duty cycle range because of the longer on-state condition for buck converters. It can be seen that both topologies have a good efficiency for all current operation because in this range of duty cycles, the input current of the converter is much higher compared to the quiescent current, so that the quiescent current impact on the efficiency is less prominent.

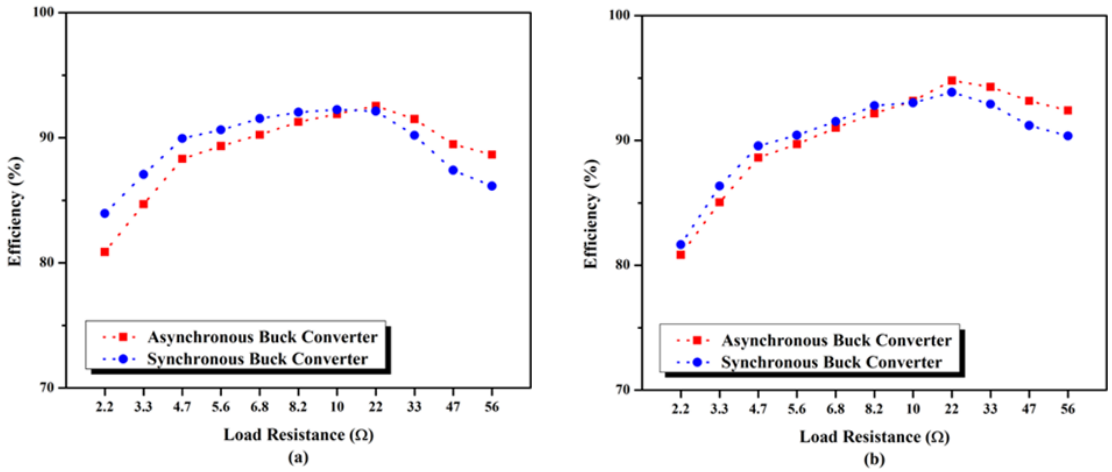

Figure 16. Load Resistance Variations on a High Duty Cycle Range: (a) Prototype Experiment 70% Duty Cycle (b) Prototype Experiment 80% Duty Cycle

Higher duty cycle range leads to a longer conduction time for the high side switch compared to the low side switch. As discussed earlier, the voltage drop of MOSFET in a low side switch for the synchronous buck converter is lower than that of the diode for the asynchronous buck converter. But because the shorter time that the low side switch conducts, the difference in voltage drop in the two topologies will become less prominent. As shown in Figure 14, the efficiency value of the synchronous topology is still higher than the asynchronous topology when the load resistance is below 22 Ω, but the differences becomes less significant.

The results of this research resembles the previous research regarding the efficiency of the synchronous and nonsynchronous buck converters for Texas Instruments converters[45]. The research shows a better efficiency of a nonsynchronous buck converter against the synchronous buck converter in lighter loads. In a higher load, the research also shows the efficiency advantage of synchronous buck converter against the nonsynchronous buck. In addition, the research also shows when the conduction time of diode is less often or can be said in a higher duty cycle range, the efficiencies of buck converters in full load were nearly the same.

6. CONCLUSIONS

The result of the experiment shows a similar characteristic of efficiency graph between the simulation model and the hardware prototypes. Nevertheless, the overall efficiency value for the simulation model is higher because the simulation does not factor in the dissipation caused by traces and wires which exists in the hardware prototypes. Furthermore, results of the proposed converter prototype showed that due to the asynchronous buck converter characteristics to operate in Discontinuous Conduction Mode, in a low current operation with the load resistance varied between 56 Ω, 47 Ω, 33 Ω, 22 Ω, it will show a higher efficiency than the synchronous buck converter in which the asynchronous buck reach overall efficiency of 83.71% against the asynchronous buck converter with overall efficiency of 78.92% for all variations of duty cycle value. Whereas in a higher current operation with the load resistance varied between 10 Ω, 8.2 Ω, 6.8 Ω, 5.6 Ω, 4.7 Ω, 3.3 Ω, and 2.2 Ω, the use of low-side switch MOSFET favors the synchronous buck converter resulting higher conversion efficiency with 87.47% efficiency against that of the asynchronous buck with 84.85% efficiency. Furthermore, in higher current operation, the synchronous buck efficiency advantage over asynchronous buck is more prominent in a low duty cycle range with 85.46% against that of the asynchronous buck with 81.32% because a longer conduction time for the low side switch, while in a higher duty cycle range, the synchronous buck converter still shows efficiency advantages but the efficiency difference is less significant with 89.48% for synchronous topology and 88.37% for asynchronous topology. Future research on asynchronous and synchronous buck converter should further investigate the efficiency comparison of both converters in real-life application, especially when the converters connected to a battery because of how crucial conversion efficiency in most of electronics devices.

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REFERENCES

[1] F. Kurniawan, Lasmadi, O. Dinaryanto, B. Sudibya, and M. R. E. Nasution, "A Novel Boost-Buck Converter Architecture for Improving Transient Response and Output-Voltage Ripple," *J. ICT Res. Appl.*, vol. 14, no. 2, pp. 149–164, 2020, https://doi.org/10.5614/itbj.ict.res.appl.2020.14.2.4.

[2] S. S. Park, J. S. Lee, and S. D. Yu, "A novel adaptive hysteresis DC-DC buck converter for portable devices," *Turkish Journal of Electrical Engineering and Computer Sciences*, vol. 27, no. 2, pp. 807-818, 2019, https://doi.org/10.3906/elk-1809-45.

[3] A. Sheikholeslami, "Buck and Boost Converters [Circuit Intuitions]," *IEEE Solid-State Circuits Mag.*, vol. 13, no. 4, pp. 12–14, 2021, https://doi.org/10.1109/MSSC.2021.3110306.

[4] S. N. Soheli, G. Sarowar, M. A. Hoque, and M. S. Hasan, "Design and Analysis of a DC -DC Buck Boost Converter to Achieve High Efficiency and Low Voltage Gain by using Buck Boost Topology into Buck Topology," *2018 International Conference on Advancement in Electrical and Electronic Engineering (ICAEEE)*, pp. 1-4, 2018, https://doi.org/10.1109/ICAEEE.2018.8643001.

[5] K. Chomsuwan, P. Prisuwanna, and V. Monyakul, "Photovoltaic grid-connected inverter using two-switch buck-boost converter," *Conference Record of the Twenty-Ninth IEEE Photovoltaic Specialists Conference*, pp. 1527-1530, 2002, https://doi.org/10.1109/PVSC.2002.1190902.

[6] T. A. C. M. Claasen, "An industry perspective on current and future state of the art in system-on-chip (SoC) technology," in *Proceedings of the IEEE*, vol. 94, no. 6, pp. 1121–1137, 2006, https://doi.org/10.1109/JPROC.2006.873616.

[7] K. Yao, Y. Meng, and F. C. Lee, "A novel winding coupled-buck converter for high-frequency, high step-down DC/DC conversion," in *PESC Record - IEEE Annual Power Electronics Specialists Conference*, vol. 2, pp. 651–656, 2002, https://doi.org/10.1109/PSEC.2002.1022527.

[8] H. H. Chou, W. H. Luo, H. L. Chen, and S. F. Wang, "A Novel Buck Converter with Dual Loops Control Mechanism," Electron, vol. 11, no. 8, p. 1256, 2022, https://doi.org/10.3390/electronics11081256.

[9] H. Sucu, T. Göktaş, and M. Arkan, "Design, Simulation and Application of Buck Converter with Digital PI Controller," *Balkan Journal of Electrical and Computer Engineering*, vol. 9, no. 2, pp. 106–113, 2021, https://doi.org/10.17694/bajece.884290.

[10] P. Barrade, "Switched-mode converters (one quadrant)," in *CAS - CERN Accelerator School and CLRC Daresbury Laboratory : Specialised CAS Course on Power Converters*, pp. 185–208, 2006, http://dx.doi.org/10.5170/CERN-2006-010.185.

[11] I. Batarseh and A. Harb, *Power Electronics*, 2nd ed. Cham: Springer, 2018, https://doi.org/10.1007/978-3-319-68366-9.

[12] P. Rajeswari and V. Manikandan, "Analysis of effects of MOSFET parasitic capacitance on non-synchronous buck converter electromagnetic emission," *Ain Shams Engineering Journal*, p. 102041, 2022, https://doi.org/10.1016/j.asej.2022.102041.

[13] J. Pathan, "Model Predictive Control of DC-DC Buck Converter and Its Comparison With Pid Controller," *International Journal of Advanced Research in Engineering and Technology*, vol. 11, no. 9, 362-367, 2020, https://ssrn.com/abstract=3713708.

[14] I. Sudiharto, M. I. Rahadyan, and O. A. Qudsi, "Design and Implementation of Buck Converter for Fast Charging with Fuzzy Logic," *JAREE (Journal on Advanced Research in Electrical Engineering)*, vol. 5, no. 1, 2021, https://doi.org/10.12962/jaree.v5i1.146.

[15] M. Rashid, *Power electronics: circuits, devices, and applications*, 3rd ed. New Jersey: Pearson, 2003.

[16] B. Bryant and M. K. Kazimierczuk, "Modeling the closed-current loop of PWM boost DC-DC converters operating in CCM with peak current-mode control," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 11, pp. 2404-2412, 2005, https://doi.org/10.1109/TCSI.2005.853904.

[17] G. Dileep and S. N. Singh, "Selection of non-isolated DC-DC converters for solar photovoltaic system," *Renewable and Sustainable Energy Reviews*, vol. 76, pp. 1230–1247, 2017, https://doi.org/10.1016/j.rser.2017.03.130.

[18] A. S. Kislovski, R. Redl, and N. O. Sokal. *Dynamic analysis of switching-mode DC/DC converters*. Springer Science & Business Media, 2012, https://doi.org/10.1007/978-94-011-7849-5.

[19] R. Abhishek, P. Zoting, and P. Ragit, "Design and Analysis of a DC -DC Buck converter and Boost Converter to Achieve High Efficiency by altering duty cycle and input voltage," *International Journal of Scientific and Research Publications*, vol. 10, no. 6, pp. 731–738, 2020, https://doi.org/10.29322/IJSRP.10.06.2020.p10285.

[20] N. B. M. Posdzi, N. B. Mahmor, and R. B. A. Rani, "Design buck converter with variable switching frequency by using matlab simulink simulation," *International Journal of Technology, Innovation, and Humanities*, vol. 1, no. 1, pp. 1–6, 2020, https://doi.org/10.29210/881201.

[21] S. Trakuldit, K. Tattiwong, and C. Bunlaksananusorn, "Design and evaluation of a Quadratic Buck Converter," *Energy Reports*, vol. 8, pp. 536–543, 2022, https://doi.org/10.1016/j.egyr.2021.11.124.

[22] O. Djekic and M. Brkovic, "Synchronous rectifiers vs. Schottky diodes in a buck topology for low voltage applications," *PESC Rec. - IEEE Annu. Power Electron. Spec. Conf.*, vol. 2, pp. 1374–1380, 1997, https://doi.org/10.1109/PESC.1997.616947.

[23] I. K. Murad, "Efficiency of Synchronous and Asynchronous Buck-Converter at Low Output Current," *Journal of University of Babylon for Engineering Sciences*, vol. 27, no. 2, pp. 194–206, 2019, https://doi.org/10.29196/jubes.v27i2.2337.

[24] O. Djekic, M. Brkovic, and A. Roy, "High frequency synchronous buck converter for low voltage applications," *PESC Rec. - IEEE Annu. Power Electron. Spec. Conf.*, vol. 2, pp. 1248–1254, 1998, https://doi.org/10.1109/PESC.1998.703166.

[25] M. Jing-Ran, Q. Yao-Jun, S. Yan-Xia, K. Shunshoku, and B. Jing, "Design of Semiconductor Synchronous Buck Converter based on GaNWide-bandgap," *Journal of Physics: Conference Series*, vol. 1486, no. 7, p. 072022, 2020, https://doi.org/10.1088/1742-6596/1486/7/072022.

[26] I. N. W. Satiawan, I. B. F. Citarsa, and I. M. B. Suksmadana, "Design and Control a High Gain Synchronous Buck Converter for a Solid State Distribution Transformer," *Journal of Physics: Conference Series*, vol. 1569, no. 3, 2020, https://doi.org/10.1088/1742-6596/1569/3/032090.

[27] H. Eraydin and A. F. Bakan, "Efficiency Comparison of Asynchronous and Synchronous Buck Converter," *Proc. - 2020 6th Int. Conf. Electr. Power Energy Convers. Syst. EPECS 2020*, pp. 30–33, 2020, https://doi.org/10.1109/EPECS48981.2020.9304966.

[28] H. Zomorodi and E. Nazari, "Design and Simulation of Synchronous Buck Converter in Comparison with Regular Buck Converter," *International Journal of Robotics and Control Systems*, vol. 2, no. 1, pp. 79–86, 2022, https://doi.org/10.31763/ijrcs.v2i1.538.

[29] N. R. Jalakanuru, "Comparative Analysis of Buck, Synchronous Buck and Modified Synchronous Buck Converters for Portable Applications," *International Journal of Science Technology & Engineering*, vol. 2, no. 5, pp. 106–111, 2015, https://ijste.org/Article.php?manuscript=IJSTEV2I5042.

[30] F. Badr, "The Effect Of Resistive Load Variations On The Open-Loop Control Of Dc-Dc Buck Converter," *Journal of Engineering and Sustainable Development*, vol. 17, no. 6, pp. 87–96, 2013, https://jeasd.uomustansiriyah.edu.iq/index.php/jeasd/article/view/1027.

[31] A. W. N. Husna, S. F. Siraj and M. H. Mat, "Effect of Load Variations in DC-DC Converter," *2011 Third International Conference on Computational Intelligence, Modelling & Simulation*, pp. 394-398, 2011, https://doi.org/10.1109/CIMSim.2011.78.

[32] S. Masri, N. Mohamad, and M. H. M. Hariri, "Design and development of DC-DC buck converter for photovoltaic application," *2012 International Conference on Power Engineering and Renewable Energy (ICPERE)*, pp. 1-5, 2012, https://doi.org/10.1109/ICPERE.2012.6287236.

[33] D. W. Gao, *Energy storage for sustainable microgrid*, Elsevier Inc., 2015, https://books.google.co.id/books?hl=id&lr=&id=VWEpBgAAQBAJ&oi=fnd&.

[34] C. Deekshitha and K. L. Shenoy, "Design and simulation of synchronous buck converter for LED application," *2017 2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT)*, pp. 142-146, 2017, https://doi.org/10.1109/RTEICT.2017.8256574.

[35] Z. Iqbal, U. Nasir, M. T. Rasheed, and K. Munir, "A comparative analysis of synchronous buck, isolated buck and buck converter," *2015 IEEE 15th International Conference on Environment and Electrical Engineering (EEEIC)*, pp. 992-996, 2015, https://doi.org/10.1109/EEEIC.2015.7165299.

[36] M. Dinesh and K. Sathish, "Design and Control of Buck Converter using PI control and Reference Regulator Technique," *International Journal on Recent Technologies in Mechanical and Electrical Engineering*, vol. 2, no. 3, pp. 46–49, 2015, https://www.ijrmee.org/index.php/ijrmee/article/view/174.

[37] A. Castaldo, *Switching regulator fundamentals-application report-switching regulator fundamentals*. Texas Instruments, Tech. Rep., 2019.

[38] G. C. Diyoke, "Analysis and Simulation Of Buck Switch Mode Dc To Dc Power Regulator," *International Journal of Technical Research & Applications*, vol. 3, no. 1, pp. 97–103, 2015, https://www.ijtra.com/abstract.php?id=analysis-and-simulation-of-buck-switch-mode-dc-to-dc-power-regulator.

[39] N. Murshed, M. S. K. Tushar, and S. Chowdhury, "Power Performance Analysis of PV Module with DC to DC Buck Converter," *Advanced Journal of Graduate Research*, vol. 8, no. 1, pp. 27–39, 2020, https://doi.org/10.21467/ajgr.8.1.27-39.

[40] S. Murmu and M. B. Sharma, "Study and Design, Simulation of PWM based Buck converter for Low Power Application," *IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)*, vol. 10, no. 4, pp. 1–17, 2015, https://www.iosrjournals.org/iosr-jeee/pages/10(4)Version-2.html.

[41] R. Khanna, "LM5033,LM5115 Analyzing Power Modules Literature Number: SNVA590," 2005.

[42] R. Lai, F. Wang, R. Burgos, D. Boroyevich, D. Zhang and P. Ning, "A Shoot-Through Protection Scheme for Converters Built With SiC JFETs," in *IEEE Transactions on Industry Applications*, vol. 46, no. 6, pp. 2495-2500, 2010, https://doi.org/10.1109/TIA.2010.2070785.

[43] T. Abuzairi, W. W. A. Ramadhan, and K. Devara, "Solar Charge Controller with Maximum Power Point Tracking for Low-Power Solar Applications," *International Journal of Photoenergy*, vol. 2019, 2019, https://doi.org/10.1155/2019/5026464.

[44] A. Rezky, K. Devara, N. S. Wardana, S. Ramadhanty, and T. Abuzairi, "Simple method for I-V characterization curve for low power solar cell using arduino nano," *E3S Web of Conferences*, vol. 67, p. 01020, 2018, https://doi.org/10.1051/e3sconf/20186701020.

[45] R. Nowakowski and N. Tang, “Efficiency of synchronous versus nonsynchronous buck converters,” 2009.

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