

A Self-Balancing 13-Level Single-Phase Triple Gain Inverter

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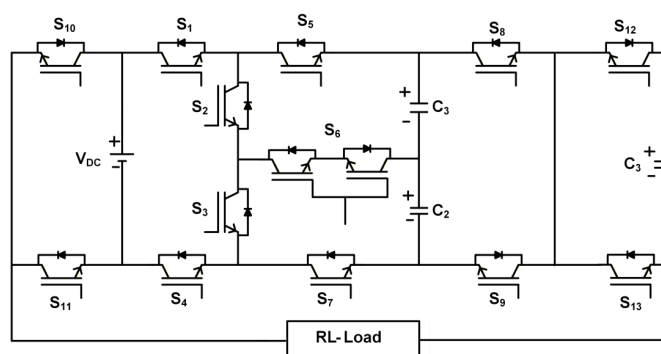
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ABSTRACT



A potential single stage power electronics interface for integrating renewable sources like PV, fuel cells, etc. with an AC load is a switched capacitor based multilevel inverter with boosting capability. In this research, a thirteen-level MLI topology with voltage boosting factor of three a gain of three for the renewable energy integration is proposed. The proposed MLI requires twelve unidirectional switches, one bidirectional switch, three capacitors, and a single DC source. The voltage stress across each switch is lower than the peak output voltage since the proposed inverter doesn't need a back-end H-Bridge. The proper selection of switching sequence enables the self regulation of voltage across all three capacitors, is self-regulated eliminating the need of additional sensor/control. Simulation results obtained from MATLAB/Simulink confirm the stable operation of the MLI and the self-regulation of switched capacitor voltages under step variations in load, source voltage, and modulation index. A comprehensive comparison with existing topologies demonstrates the superiority of the proposed topology in terms of reduced total number of components and lower total blocking voltage.

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1. INTRODUCTION

The use of renewable energy sources, such as solar photovoltaic systems, wind energy conversion systems, and fuel cells, requires effective DC to AC conversion. Multilevel inverters, owing to their intrinsic benefits such as decreased dv/dt , decreased voltage stress across the switch, enhanced voltage and current THD, fault-tolerant operation, and decreased common mode voltage, have been suggested for the above-mentioned applications [1]-[6]. Diode clamped multilevel inverters, flying capacitor multilevel inverters, and cascaded H-bridge multilevel inverters are some of the common multilevel inverter topologies [7]-[8]. The primary drawback of standard multilevel inverter topologies is that as the number of levels increases, more number of components become necessary [9].

RDC multilevel inverters employing a single source, reduced source, and switched capacitors without boosting capacity have been described [10]-[16]. Research articles [11]-[15] have discussed in-depth comparisons of various multilevel inverters with fewer devices. However, a common drawback of traditional MLI and RDC MLI is that they can only produce an output voltage that is less than or equal to the input voltage. To overcome this drawback various switched capacitor based boost inverters have been introduced [17]-[32]. The various existing 13-level single-phase MLI with triple voltage gain were discussed in [33]-[36]. Another thirteen level inverter with gain of 1.5 and gain of 6 is briefed in [37]-[39]. A generalized switched capacitor module was proposed in [33] which was combined with a packed H-bridge structure to produce a 13-level output using two sources. The major drawback of this topology is that it requires two supply sources, a higher total blocking voltage and four capacitors to realize a 13-level output across the load. A generalized step-up MLI using crisscross capacitor units was suggested in [34]. Two crisscross units are required for a voltage gain of 3. The main issues are that it requires 4 capacitors and a mix of semiconductor switches with a freewheeling diode and without a freewheeling diode to realize a thirteen level output. A new 13-level MLI was proposed in [35] with less total blocking voltage. But the topology requires 4 additional diodes and 4 switched capacitors to realize 13-level output. The increased number of other components in [35] results in less reliability. A 12-switch based 13-level SC-MLI with the gain of three is proposed in [36]. In addition to power semiconductor switches it requires 3 capacitors and 3 diodes. Decreased efficiency at high power and use of additional diodes are the main problem with the topology [36]. A single source thirteen level K-type MLI is proposed in [37], which requires 4 capacitors to realize thirteen level output with gain of 1.5. It requires mix of semiconductor switch with freewheeling diode and without freewheeling diode. In general, from the above literature study there is need of single source MLI with reduced number of switches and other components such as capacitors and diodes so as increase the reliability efficiency and power density of inverter. This paper therefore introduces a switched capacitor-based MLI topology that achieves gain of three with reduced number of capacitors and incorporates LDN topology to achieve more number voltage levels using fewer switches. The key features of this proposed topology include:

- Utilization of a single DC voltage source
- Only 14 switches are needed to produce a 13-level output (Bidirectional switches are counted as two unidirectional switches while arriving total number of switches)
- A gain of 3
- The maximum voltage stress is limited to $2V_{DC}$
- An inherent polarity converter that eliminates the need for a backend H-bridge
- Capacitors are self-balancing, negating the requirement for external sensors.

The rest of the paper is organized as follows: The Section-2 describes the circuit diagram of the proposed topology and its operation. In Section-3 the modulation technique adopted to generate gate pulse is described. The Section-4 describes the Level Doubling Network's self-balancing characteristic along with mathematical expressions. In Section 5, simulation findings under steady and dynamic conditions are provided. In Section 6, we highlight the superiority of this topology over the existing topology and Section-7 summarizes the conclusions of the proposed work.

2. CIRCUIT DESCRIPTION

The schematic representation of the proposed boost multilevel inverter topology is depicted in [Figure 1](#). The innovative features of this topology include the requirement of only a single DC source (V_{DC}), a boosting factor of three, an integrated polarity generator, and a maximum voltage stress across the switch that is lower than the maximum output voltage. The input DC source can be derived from a fuel cell, battery, or solar PV system. Utilizing the proposed inverter, the following 13 levels can be generated: ($\pm 3V_{DC}, \pm 2.5V_{DC}, \pm 2V_{DC}, \pm 1.5V_{DC}, \pm V_{DC}, \pm 0.5V_{DC}, 0V_{DC}$). The proposed inverter consists of 12

unidirectional switches, 1 bidirectional switch, and 3 capacitors. Among the 12 unidirectional there are three pairs of complimentary switches (S_8 & S_9, S_{10} & S_{11}, S_{12} & S_{13}).

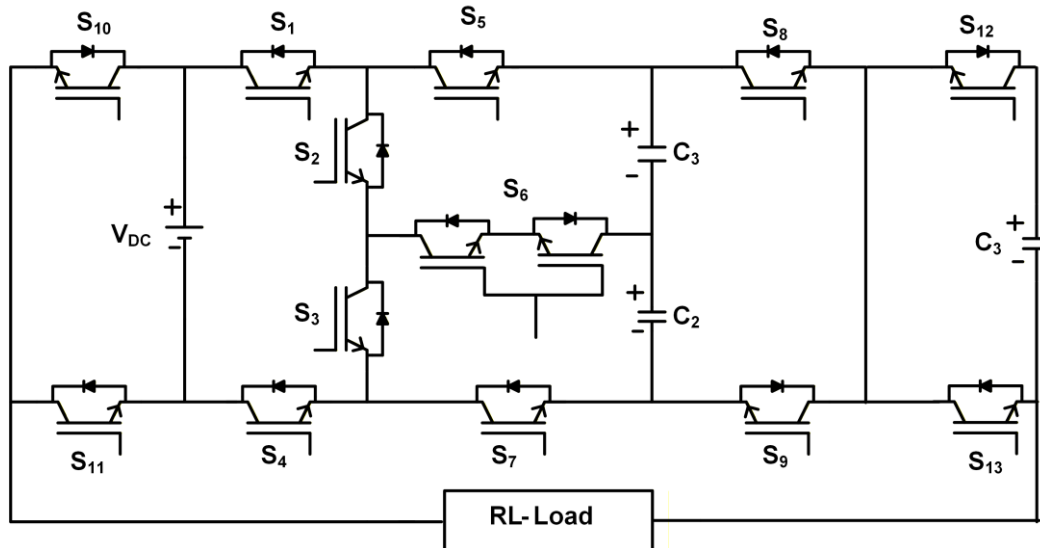


Figure 1. Structure of proposed topology

The complementary switches must not be activated at the same time to prevent a short circuit of the capacitor or source. The switches S_8 and S_9 operate at the fundamental switching frequency. The switch S_6 is a bidirectional switch realized using a common-emitter configuration, as it offers reduced gate-drive requirements and comparatively lower on-state losses. There are three capacitors: two boost capacitors (C_1 and C_2) and one level-doubling capacitor (C_3). The boosting capacitor is connected in parallel to the DC source during the charging phase and in series during the discharging phase. Consequently, the voltage of the boosting capacitors is regulated to match the supply voltage, V_{DC} . The voltage of the level-doubling capacitor is adjusted to be half of the supply voltage by charging and discharging it for equal intervals within one fundamental cycle. As the voltage across the three capacitors is self-regulated, external sensors are not required to achieve this regulation. The various switching states of the proposed inverter are detailed in Table 1. Switches S_1 , to S_4, S_{10} to S_{11} and S_6 is subject to voltage stresses of V_{DC} , switches S_5 and S_7 to S_9 experience a blocking voltage of $2V_{DC}$, and switches S_{12} and S_{13} are subject to a voltage stresses of $\frac{V_{DC}}{2}$ under blocking condition.

Table 1. Switching States of various levels

Switches/Voltage Level	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_{10}	S_{12}	C_1	C_2	C_3
$+3 V_{DC}$	1	1	1	0	0	0	1	1	0	0	↓	↓	-
$+2.5 V_{DC}$	1	1	1	0	0	0	1	1	0	1	↓	↓	↓
$+2 V_{DC}$	1	1	0	1	0	1	1	1	0	0	↓	↑	-
$+1.5 V_{DC}$	1	1	0	1	0	1	1	1	0	1	↓	↑	↓
$+1 V_{DC}$	1	0	1	1	1	1	0	1	0	0	↑	-	-
$+0.5 V_{DC}$	1	0	1	1	1	1	0	1	0	1	↑	-	↓
$+0 V_{DC}$	1	0	1	1	1	1	0	1	1	0	↑	-	-
$-0 V_{DC}$	1	1	0	1	0	1	1	0	0	0	-	↑	-
$-0.5 V_{DC}$	1	1	0	1	0	1	1	0	0	1	-	↑	↑
$-1 V_{DC}$	1	1	0	1	0	1	1	0	1	0	-	↑	-
$-1.5 V_{DC}$	1	1	0	1	0	1	1	0	1	1	↑	↓	↑
$-2 V_{DC}$	1	0	1	1	1	1	0	0	1	0	↑	↓	-
$-2.5 V_{DC}$	1	0	1	1	1	1	0	0	1	1	↓	↓	↑
$-3 V_{DC}$	0	1	1	1	0	0	0	0	1	0	↓	↓	-

Information: “↑”=Charging, “↓”=Discharging, “-”= not affected

3. SINGLE CARRIER BASED MODULATION METHOD

Various methods have been proposed in literature to generate gate pulse for the multilevel inverter [40]–[42]. The performance of the proposed topology is analyzed with the help of single carrier based sinusoidal pulse width modulation proposed in [43] owing to its simplicity, easy implementation and reduced number of comparators compared to conventional level-shifted and phase-shifted PWM schemes. To generate gate pulse

for thirteen level inverters using this modulation technique requires single carrier signal ($V_{carrier}$) and six reference signals ($V_{ref1}, V_{ref2}, V_{ref3}, V_{ref4}, V_{ref5}, V_{ref6}$). The schematic of the modulator is illustrated in Figure 2. The modulation index (M_a) for thirteen-level inverter is defined to be as per [43].

$$M_a = \frac{A_m}{6 * A_c} \quad (1)$$

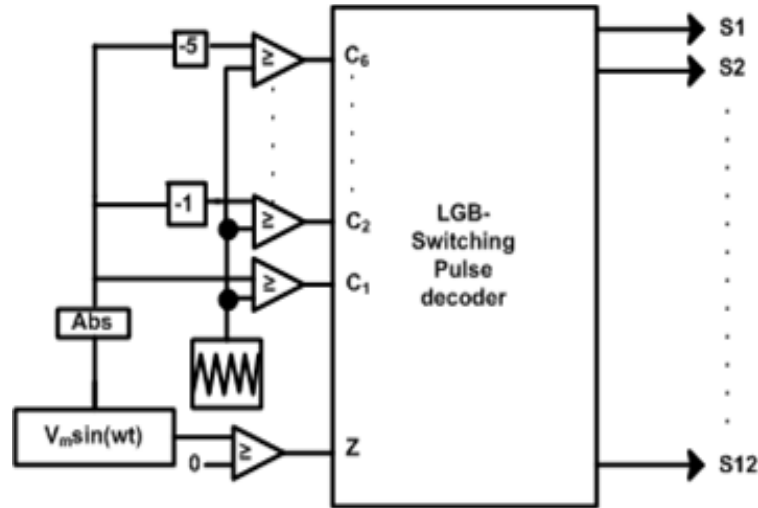


Figure 2. Logic Gate Based Switching Pulse Decoder

In the equation (1), A_m is the Peak amplitude of modulating signal and A_c is the Peak amplitude of carrier signal. All the reference signals are rectified sinusoidal waveforms which are in phase with each other with same frequency and amplitude depending on the required modulation index, but each are offset by a value that is equivalent to the amplitude of the carrier signal. Each of the reference signals is compared with the carrier waveform and six outputs (C_1 to C_6) are obtained. Also, a signum function (Z) is generated to indicate the positive and negative cycle of the reference waveform. The signum function output is 1 when the reference sinusoidal signal is greater than equal to zero else its output is zero. By applying suitable logic operation of the comparator outputs and signum function particular level information is obtained. The gating pulses for each switch are determined based on the switching states in which they are to be activated, as outlined in Table 1. For example, the switch S_8 is turned for entire positive half cycle, hence the logic equation for gating signal is given by,

$$S_8 = z \quad (2)$$

In same manner the Boolean expressions for the remaining independent switches are given by.

$$S_1 = Z + (\sim C_1 Z) + (C_1 \sim C_6 Z) \quad (3)$$

$$S_2 = (\sim C_1 \sim Z) + (C_3 Z) + (C_1 \sim C_4 \sim Z) + (C_6 Z) \quad (4)$$

$$S_3 = (C_5 Z) + (C_1 \sim C_3 Z) + (\sim C_1 Z) + (C_4 \sim Z) \quad (5)$$

$$S_4 = (C_1 \sim C_5 Z) + (\sim C_1 Z) + \sim Z \quad (6)$$

$$S_5 = (C_1 \sim C_3 Z) + (\sim C_1 Z) + (C_4 \sim Z) \quad (7)$$

$$S_6 = (C_1 \sim C_5 Z) + (\sim C_1 Z) + (\sim C_1 \sim Z)(C_1 \sim C_6 \sim Z) \quad (8)$$

$$S_7 = (C_3 \cdot Z) + (\sim C_1 \sim Z) + (C_1 \sim C_4 \sim Z) + (C_6 Z) \quad (9)$$

$$S_{10} = (\sim C_1 Z) + (C_2 \sim Z) \quad (10)$$

$$S_{12} = (C_1 \sim C_2) + (C_3 \sim C_4) + (C_5 \sim C_6) \quad (11)$$

Switches S_8 and S_9 , S_{10} and S_{11} , and S_{12} and S_{13} are complementary to each other hence a NOT gate is used in the output of S_8, S_{10}, S_{11} to generate gate pulse for S_9, S_{11} and S_{13} respectively.

4. SELF BALANCING OF CAPACITOR

The self-balancing of the LDN capacitor C_3 is accomplished by ensuring it charges and discharges for the same duration within a single fundamental cycle. In this proposed topology, the LDN capacitor discharges during the positive half cycle and charges during the negative half cycle. As the capacitor is charged and discharged for equal interval, the net charge associated with it zero. The charging and discharging current associated with LDN capacitor with load impedance of Z_L are given as per the following equations,

$$I_c^+_{(+2.5V_{DC})} = \left(\frac{2V_{DC} + V_C}{Z_L} \right) \quad (12)$$

$$I_c^+_{(+1.5V_{DC})} = \left(\frac{V_{DC} + V_C}{Z_L} \right) \quad (13)$$

$$I_c^+_{(+0.5V_{DC})} = \left(\frac{V_C}{Z_L} \right) \quad (14)$$

$$I_c^-_{(-0.5V_{DC})} = \left(\frac{V_{DC} - V_C}{Z_L} \right) \quad (15)$$

$$I_c^-_{(-1.5V_{DC})} = \left(\frac{2V_{DC} - V_C}{Z_L} \right) \quad (16)$$

$$I_c^-_{(-2.5V_{DC})} = \left(\frac{3V_{DC} - V_C}{Z_L} \right) \quad (17)$$

$$Q_{net} = \left[\frac{6V_C - 3V_{DC}}{Z_L} \right] T \quad (18)$$

$$V_C = \frac{V_{DC}}{2} \quad (19)$$

From the expression (19), it is proved that the voltage across the LDN capacitor is regulated to $\frac{V_{DC}}{2}$.

4.1. DESIGN OF CAPACITANCE

The values of boost capacitors (C_1, C_2) are designed based on the longest discharging interval (LDI). For boost capacitor (C_1), the LDI occurs during the positive half of the output voltage and for capacitor (C_2) the LDI occurs during the negative half of the output voltage as evident from the Figure 3. As the LDI of both the boost capacitors are same both have same capacitance value. Hence the capacitance computation for (C_1) alone is briefed in detail. The capacitance value for (C_1) is arrived based on the charge associated with it

during the LDI. The charge associated with the capacitor is, where a to b is the LDI of the capacitor (C_1), I_m is the peak load current.

$$\Delta Q_c = \frac{1}{\omega} \int_{\theta_3}^{\theta_{10}} I_m \sin(\theta - \phi) d\theta \tag{20}$$

$$= \frac{1}{\omega} \int_{\theta_3}^{\theta_{10}} I_m \sin(\theta - \phi) d\theta \tag{21}$$

$$= \frac{1}{\omega} \int_{\theta_3}^{\frac{\pi}{2}} I_m \sin(\theta_3 - \phi) d\theta \tag{22}$$

$$= \frac{2I_m}{\omega} (\cos(\theta_3 - \phi) - \sin(\phi)) \tag{23}$$

where t_3 is calculated by,

$$\theta_3 = \omega t_3 = \sin^{-1}\left(\frac{A_c}{3A_m}\right) \tag{24}$$

$$C = \frac{\Delta Q_c}{\Delta V} > \frac{2I_m(\cos(\theta_3 - \phi) - \sin \phi)}{0.1V_{DC}\omega} \tag{25}$$

The capacitance value is designed by assuming the power factor of 0.85. By substituting the load of 50Ω , $120mH$ for a ripple 10% of V_{DC} the minimum capacitance required is $2200\mu F$.

4.2. DESIGN OF LDN CAPACITANCE

The charging and discharging of the LDN capacitor are illustrated clearly in Figure 3. As per this, the capacitor charges in negative half cycle and discharges at positive cycle at specific intervals also remains idle in some intervals. The capacitance value of LDN capacitor is arrived based on the procedure and equations as mentioned in [44]. The minimum value of capacitance required is found to be $2200\mu F$.

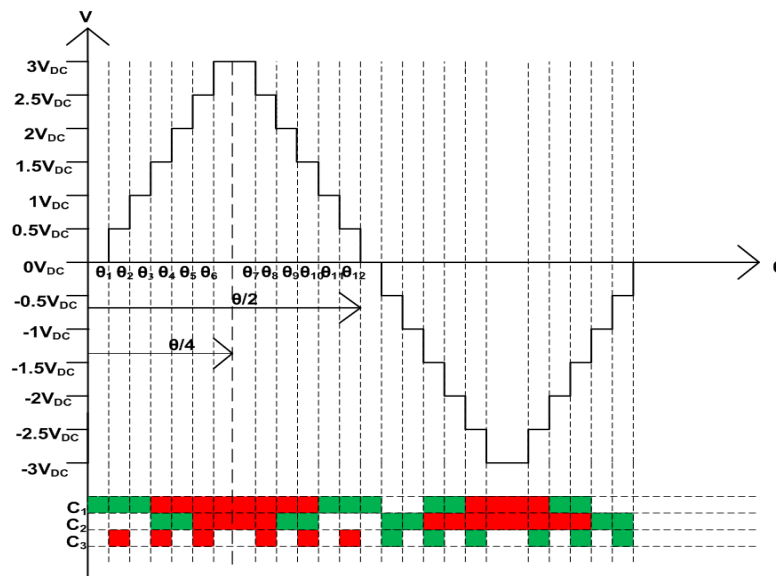


Figure 3. Charging and Discharging states of Switched capacitors

5. SIMULATIONS AND RESULTS

To assess the proposed topology's performance, a simulation model is developed using MATLAB SIMULINK. The simulation parameters used in this research are specified in Table 2. Gate pulses for each switch are generated through single carrier-based SPWM, as described in section 3. Figure 4 shows the inverter's output voltage and current waveform in a steady state. The peak output voltage across the load reaches approximately 360V for an input of 120V, confirming the proposed inverter's boosting capability.

Figure 5 and Figure 6 depict the steady state voltage across the boost capacitor and LDN capacitor, respectively. The voltage across the boost capacitors is controlled at 120V, while the LDN capacitor is kept at 60V, with voltage ripple of around 10%.

Table 2. parameters used in Simulation

Parameters	Values/Ratings
V_{DC}	120V
C_1, C_2, C_3	2200 μ F
Load	50 Ω -120mH
Output Frequency	50Hz
Carrier Frequency	5kHz
Modulation Index	0.95

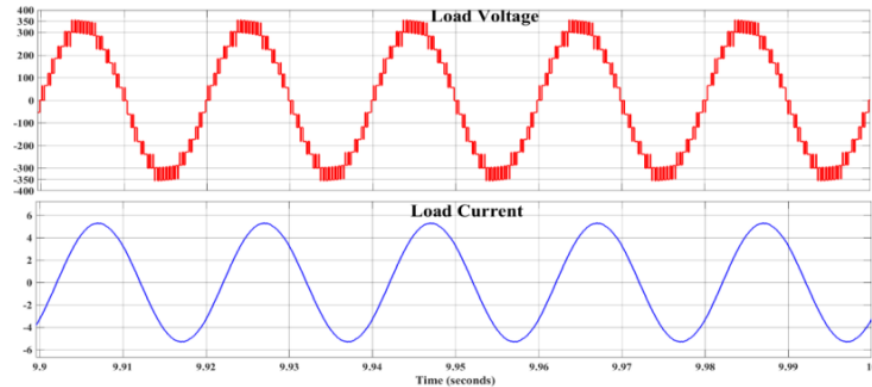


Figure 4. Load voltage and load current for load R=50 Ω and L=120mH

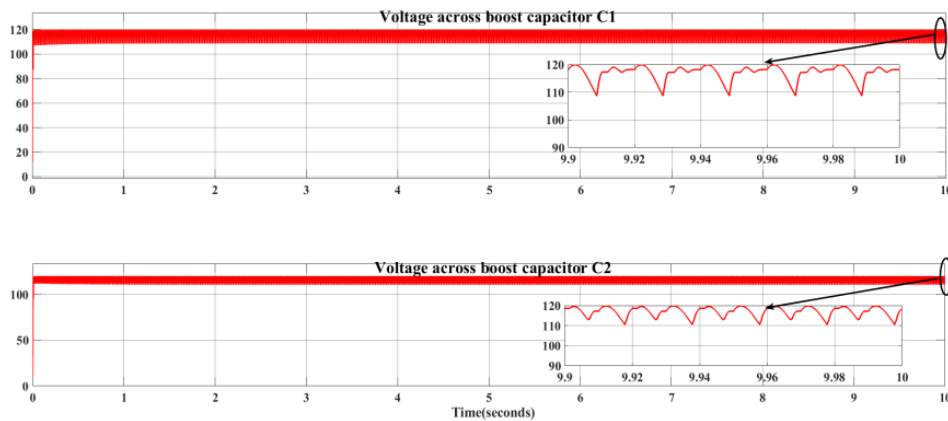


Figure 5. Voltage across Boost capacitors at steady state

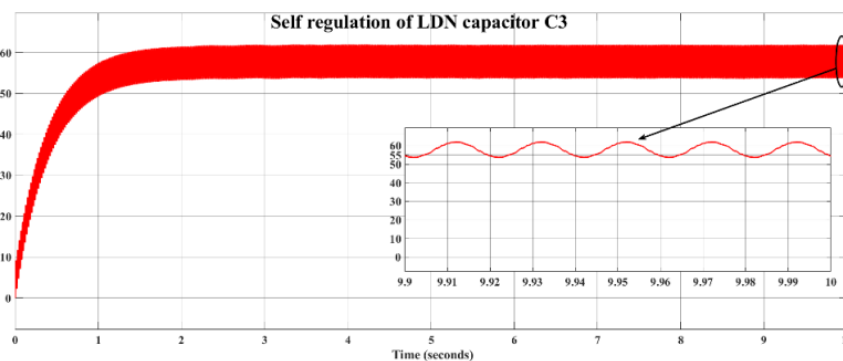


Figure 6. Voltage across LDN capacitor at steady state

To test the effectiveness of self-balancing of capacitors under dynamic condition such as step change in input voltage, load and modulation index are considered in the present study. Figure 7 shows the load voltage

and load current during the step change in input voltage. Initially the load voltage is kept as 100V and at time $t = 5$ seconds the input voltage is changes to 120V, the voltage across the boost capacitor is regulated to supply voltage and voltage across the LDN capacitor is regulated to half the supply voltage with allowable ripple as illustrated in Figure 8 and Figure 9 respectively. Figure 10 to Figure 12 shows the load voltage, current and self-regulation of capacitors for the dynamic change in load conditions from $R = 50\Omega$ to RL load with $R = 50\Omega$ and $L = 120mH$. During step change from R-load to RL-load, the voltage ripple of capacitors is reduced. According to equation (24) R-load is worst case as far as the ripple across the capacitors, which is validated in the simulation study through the Figure 11 and Figure 12.

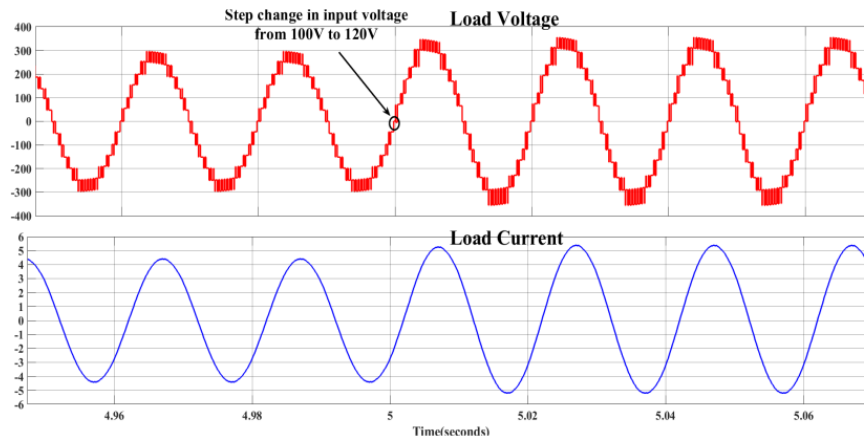


Figure 7. Load voltage and current during step change in source voltage

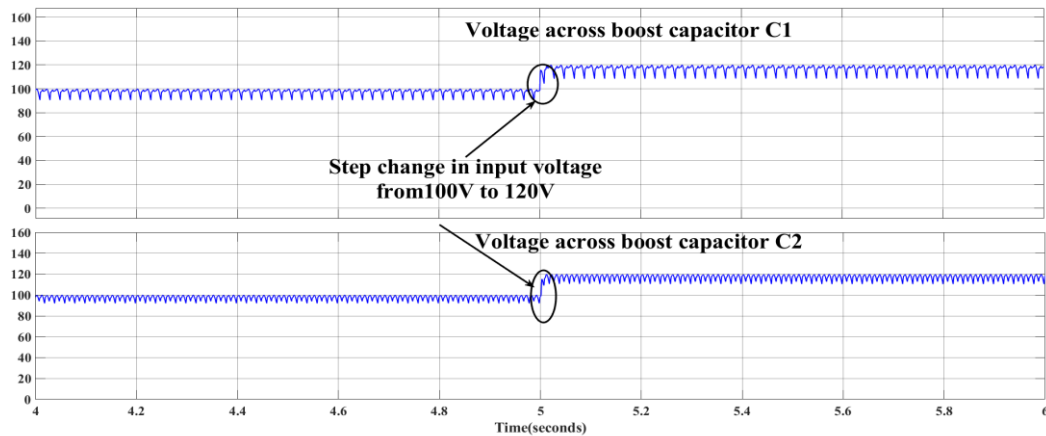


Figure 8. Voltage across Boost capacitors during step change in source voltage

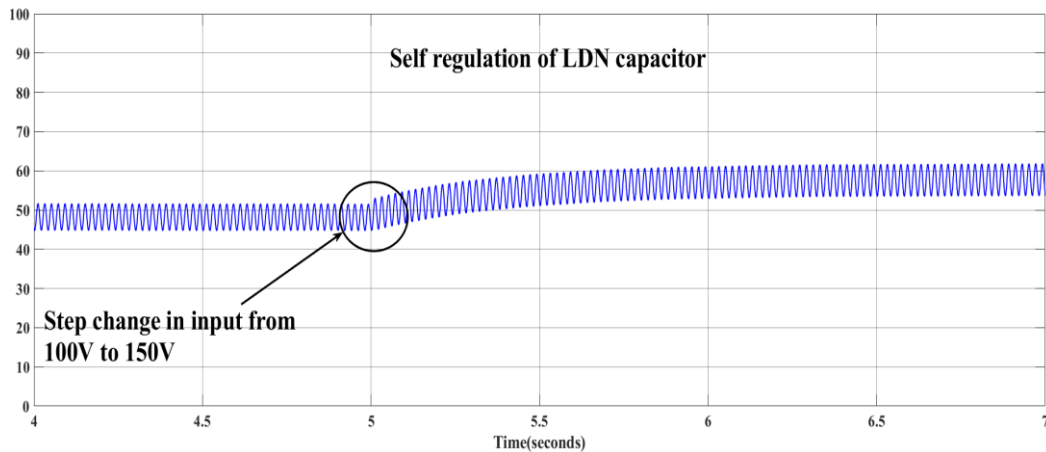


Figure 9. Voltage across LDN capacitors during step change in source voltage

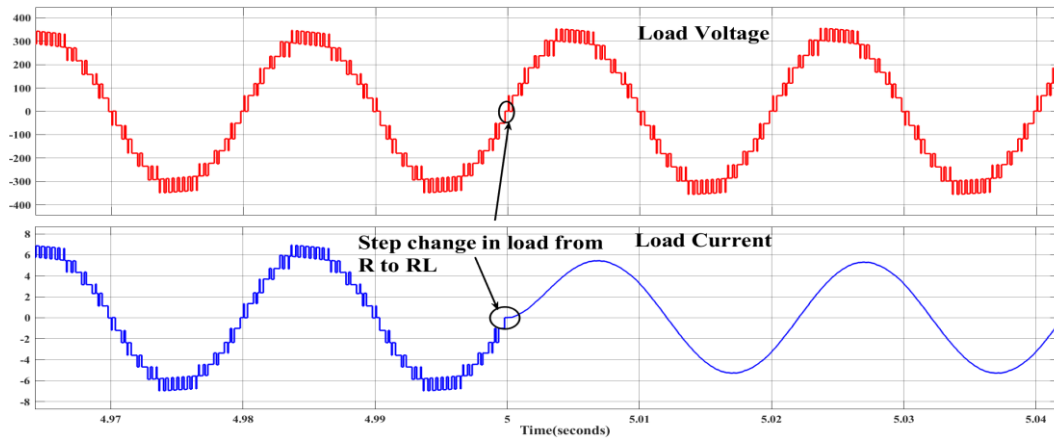


Figure 10. Load voltage and current during dynamic change in load

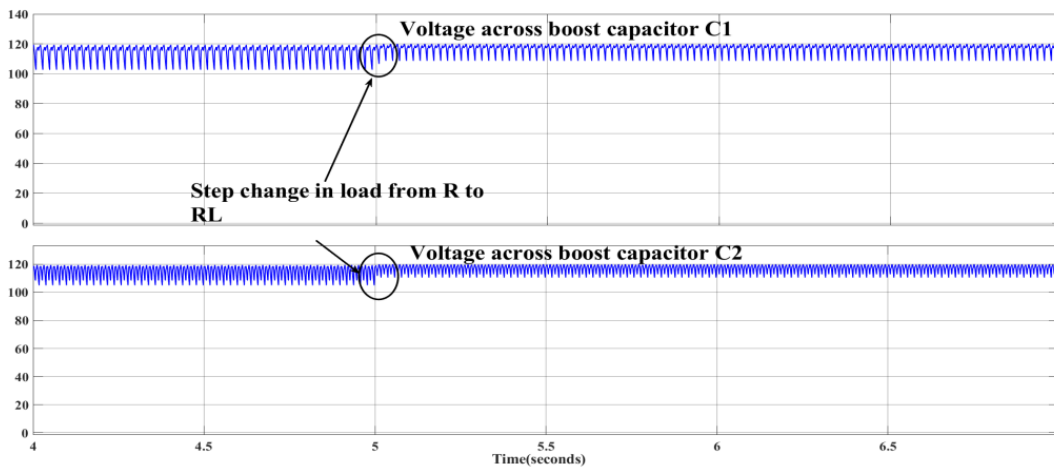


Figure 11. Voltage across Boost capacitors during dynamic change in load

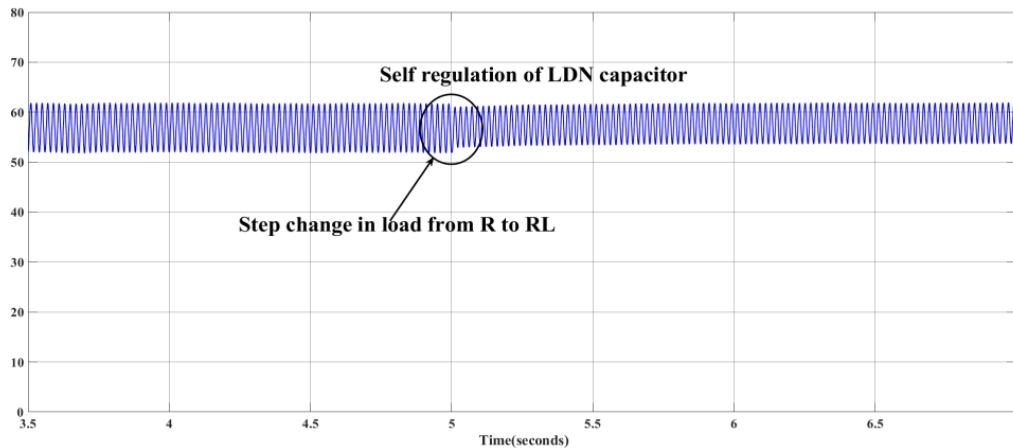


Figure 12. Voltage across LDN capacitor during dynamic change in load

The Figure 13 shows the load voltage and load current with a peak of magnitude of 300V and 4.9A respectively for the modulation of 0.8. Also, the voltage across the boost capacitor and LDN capacitor can be observed with reduced ripples as shown in the Figure 14 and Figure 15. Figure 16 shows the FFT analysis of the output voltage of the proposed topology. The THD of the output voltage is 10.85% for a modulation index of 0.95. The magnitude of the lower order harmonics is less than 1.5%, which simplifies the design of external filters. Furthermore, the load current THD is 0.81%, as shown in Figure 17, which is well below the limit prescribed by IEEE Std. 519-2022.

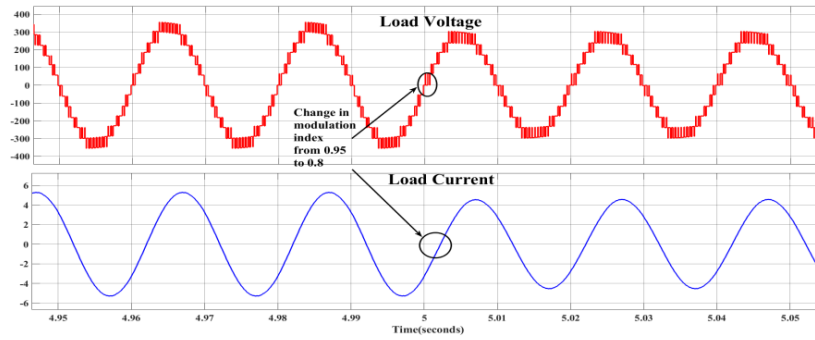


Figure 13. Load voltage and current during change in modulation index

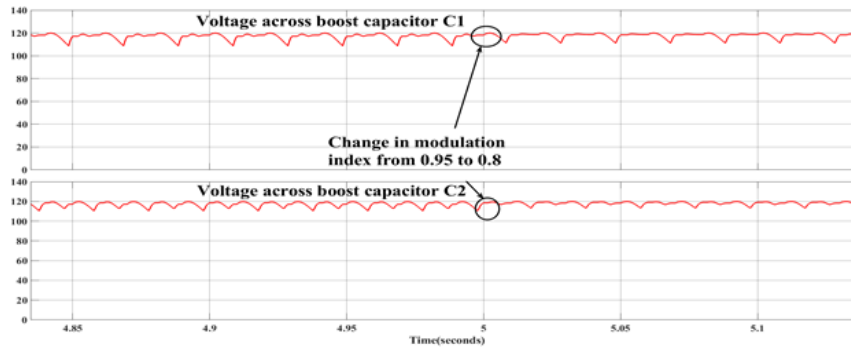


Figure 14. Voltage across Boost capacitors during change in modulation index

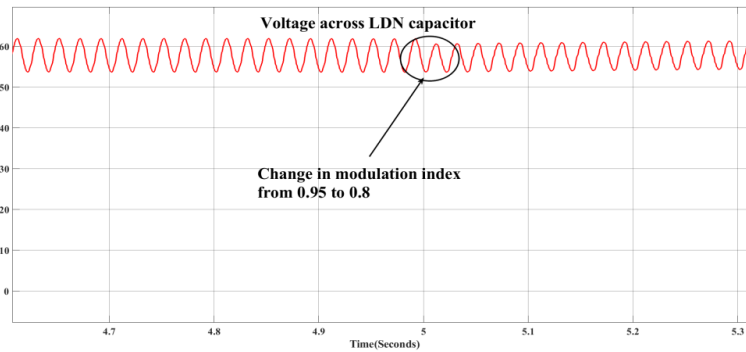


Figure 15. Voltage across LDN capacitor during change in modulation index

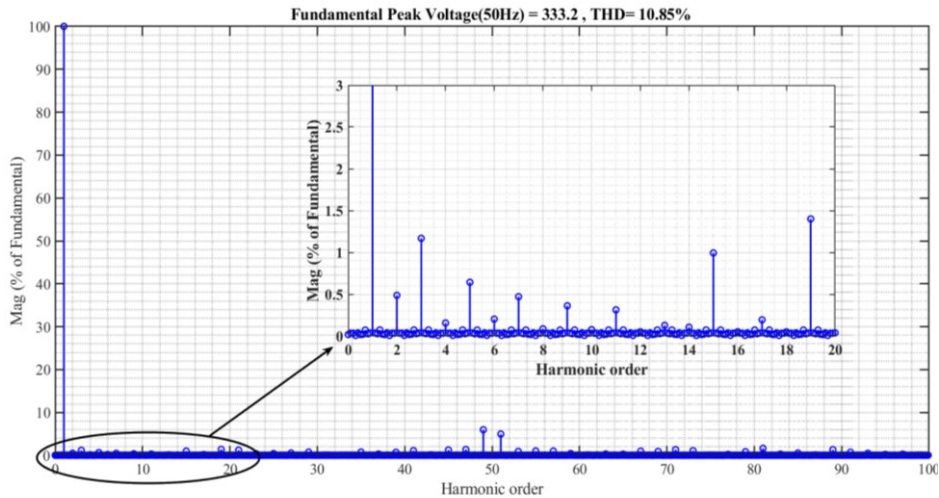


Figure 16. THD content of load voltage at steady state

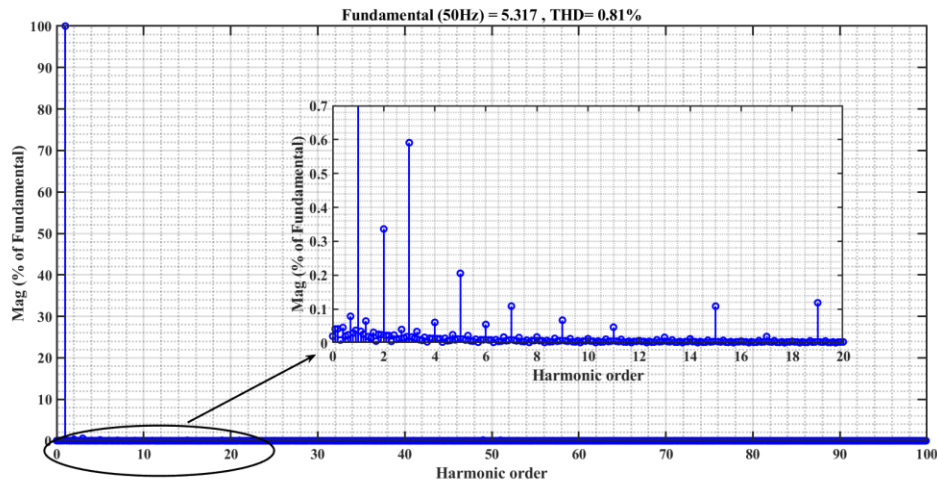


Figure 17. THD content of load current at steady state

6. COMPARATIVE ASSESSMENT

The performance comparison is evaluated based on various components, including DC sources, switches, additional diodes, and capacitors to achieve different voltage levels and obtain the desired outcomes. These parameters are compared in Table 3. The sum of switches (N_{SW}), diodes (N_D), drivers (N_{GD}), capacitors (N_{CAP}), and total blocking voltage (TBV) of the converter multiplied by the number of DC (V_{DC}) sources used constitutes the cost function of the inverter. This ratio is then multiplied by the number of voltage levels obtained. The value 1 is used in the computation to denote α , indicating that the input source voltage is equivalent to it. The expression for the cost function is articulated as follows,

$$\text{Cost Factor}(C.F) = \frac{[N_{CAP} + N_{GD} + N_{SW} + N_D + \alpha(TBV)] * N_{DC}}{N_{Levels}} \quad (25)$$

Where N_{DC} is the number of DC sources used. $MBV(*V_{DC})$ - Maximum Blocking Voltage when the switch is in OFF condition; $TBV(*V_{DC})$ -Total Blocking Voltage; N_{CS} – Max number of conducting switches.

Table 3. Comparison of prop. Topology with similar existing topology

Ref	[33]	[34]	[35]	[36]	[37]	Proposed
V_{DC}	2	1	1	1	1	1
N_{SW}	16	16	12	12	12	14
N_{GD}	16	17	11	11	11	13
N_D	2	0	4	3	0	0
N_{CAP}	4	4	4	3	4	3
N_{CS}	7	10	6	6	7	8
Gain	3	3	3	3	1.5	3
TBV	34	15.5	13	24	18	17
MBV	6	2	2	2	2	2
CLF	2.92	2.84	2.46	2.30	2.15	2.38
C.F	10.76	4.03	3.4	4.07	3.46	3.6

The proposed circuit utilizes only one DC source to produce a 13-level output, which sets it apart from Multilevel Inverter (MLI) topology [33] that require multiple DC sources. This significantly reduces the number of voltage sources required, resulting in a more simplified and efficient design. Moreover, the proposed topology requires only 14 switches, which is second best among the recent topologies proposed in the literature. This reduction in the number of switches increases the reliability and decreases losses of the proposed topology. Additionally, the number of gate drivers required for this topology is only 13, whereas other topologies like [33] require 16 gate drivers respectively, further reducing the complexity of the proposed design. Another advantage of the proposed topology is that it does not require any additional diodes, which distinguishes it from other topologies like [33],[35][36], which require 2, 4 and 3 diodes respectively. This feature reduces the complexity and losses of the proposed design. The number of capacitors used in this topology is also minimal, only 3, compared to the other topologies like [33]-[35] and [37] which require 4 capacitors. In terms of blocking voltage of switches, the proposed topology has a Total Blocking Voltage (TBV) of 17, which is lower compared to topologies like [33],[36], and [37], which have TBVs of 34, 24,

and 18 respectively. However, the Maximum Breakdown Voltage (MBV) of the proposed topology is only 2, which is less than the topology [33], which has an MBV of 6. Finally, the cost function calculated for the proposed topology is only 3.6, which is less than the cost functions of other topologies like [33]-[34] and [36]. Even though the cost factor of [35] is less than the proposed inverter it has a higher CLF which makes it less reliable on account of higher component count. The voltage gain of [37] is 1.5 only. Thus, the proposed topology offers a simple, efficient, and cost-effective solution for applications where reliability is important.

7. CONCLUSION

This paper presents a thirteen-level multilevel inverter employing an LDN topology with a reduced number of devices, achieving an output voltage boosting factor of three. The paper provides a comprehensive description of the circuit topology, details the associated switching states, and presents the capacitance design methodology for a given load condition. The capacitors used in the proposed MLI are self-balanced, eliminating the need for auxiliary control methods or additional sensors, thus simplifying control complexity. The simulation results demonstrate the inherent boosting capability and operability of the proposed topology under various test scenarios, including changes in source, load, and modulation index. The proposed topology employs only three capacitors and eliminates the need for clamping diodes, resulting in a low cost factor and making it a superior alternative to existing topologies. The strong agreement between the theoretical analysis and the simulation results confirms the topology's potential as a compact and efficient solution for renewable energy integration. Also, the future work will involve constructing a hardware prototype to validate the performance under real-world conditions.

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